FMC-1000

V 0.97 11/24/2014

FMC Module with 2x 1250 Msps 14-bit A/D, 2x 1230 Msps 16-bit D/A Converters with PLL and Timing Controls

FEATURES

- Two A/D Inputs
  - Up to 1250* Msps,14-bits each
  - AC or DC coupled
- Two D/A Outputs
  - Up to 1230* Msps,16-bits each 1x, to 2500* Msps with 4x interpolation
  - AC or DC coupled
- Sample clocks and timing and controls
  - Both front panel and FMC ports; DCLK, SYSCLK inputs, Trig/Sync/Monitor input/output, HW customizable
  - Programmable PLL
  - 25 MHz TCXO Reference
  - Integrated with FMC triggers
- FMC module, VITA 57.1
  - High Pin Count,
  - JESD204B (subclass 1) Interfaces
  - 2.5V Vadj
  - Power monitor and controls
- 10.4W typical (AC-coupled inputs)
- Conduction cooling supported
- Environmental ratings for -40 to 85C
  9g RMS sine, 0.1g2/Hz random vibration

APPLICATIONS

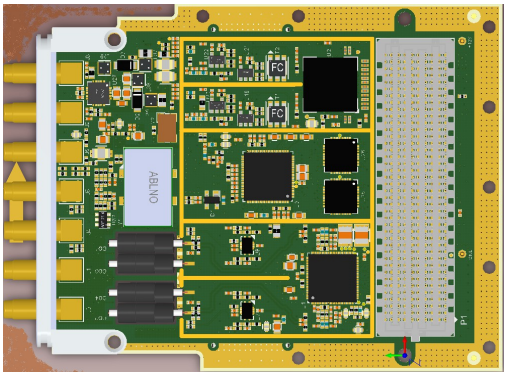
- Wireless Receiver and Transmitter
- LTE, WiMAX Physical Layer
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback

SOFTWARE

- MATLAB/VHDL FrameWork Logic

MATLAB®

XILINX®



DESCRIPTION

The FMC-1000 is a high speed digitizing and signal generation FMC I/O module featuring two 1250* MSPS A/D channels and two 1230* MSPS D/A channels supported by sample clock and triggering features.

Analog I/O may be either AC or DC coupled. The sample clock is from either an ultra-low-jitter PLL or can be derived from external inputs. Multiple cards can be synchronized for sampling.

The FMC-1000 power consumption is less than 10.4W for typical operation. The module may be conduction cooled using provided thermal interfaces and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

Support logic in VHDL is provided for integration with FPGA carrier cards. Specific support for Innovative carrier cards includes integration with Framework Logic tools that support VHDL/Verilog and Matlab developers. The Matlab BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator for the FMC integrated with the FPGA carrier card.

Software tools for Innovative carrier cards include include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features are provided.

* Sampling rates in an application depend on carrier and system design

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This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part No.	Description
FMC-1000	80325-4-<ER>	FMC module with two 1250 MSPS 14-bit A/Ds, two 1230 MSPS D/As, PLL and timing controls, AC-coupled A/D and D/As
FMC-1000	80325-5-<ER>	Like 80xxx-0 except A/Ds and D/As are DC-coupled
Cables		
SSMC to BNC cable	67156	IO cable with SSMC (male) to BNC (male), 1 meter
Carrier Cards		
PEX6-COP	80284-x-<ER>	Desktop/server PCI Express FPGA co-processor card with FMC site
Embedded Computer Hosts		
ePC-K7	90502-x-<ER>	ePC-K7, I7 CPU, K325/410-T2 Commercial FPGA. Embedded PC with support for two FMC modules; i7 quad core COM Express Type 6 CPU; Windows/Linux drivers
Mini-K7	90600-x-<ER>	Mini-K7, I7 CPU, K325/410-T2 Commercial FPGA. Embedded PC with support for one FMC modules; Atom dual core COM Express Type 6 CPU; Windows/Linux drivers

<ER> corresponds to the Environmental Rating, L0...L4.

Physicals	
Form Factor	FMC VITA 57.1 single-width
Size	76.5 x 69 mm 10 mm mounting height
Weight	180g (approximate, contact factory if critical to application)
Hazardous Materials	Lead-free and RoHS compliant

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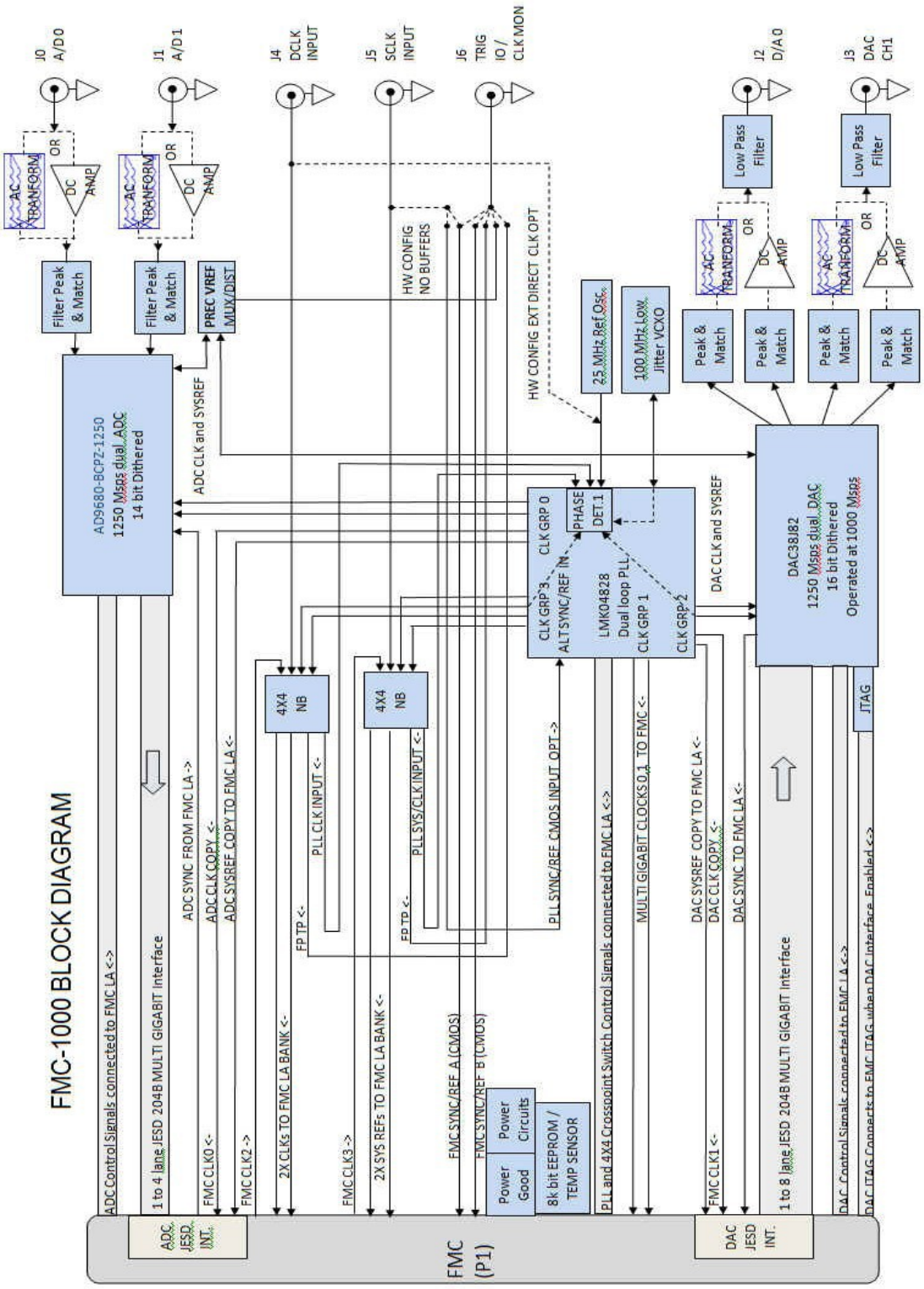

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Front Panel (Bezel) Detail

Front Panel Label	Schematic reference	Description
A/D 0	J0	A/D analog input 50 Ohm nominal impedance AC or DC coupled by model
A/D 1	J1	A/D analog input 50 Ohm nominal impedance AC or DC coupled by model
DCLK IN	J4	Logic input, 1.25V +/- 0.1V threshold, nominal range 0V to 2.5V, high impedance, DC coupled with an approximately10 kOhm pull down in standard configuration. Can be hardware configured for different threshold voltages from 0.15 to 2.35V, as AC or DC coupled, with or without a termination. The standard hardware configuration connects this to a 4X4 non-blocking cross-point switch allowing multiple uses as a clock reference or trigger routed to the FMC-1000 PLL and the carrier. Also this input can be hardware configured as direct PLL clock input (CLKin1) which can be used as a PLL input/reference or simply distributed (no PLL) for use as the FMC-1000 sampling clock.
SCLK IN	J5	Logic input, 1.25V +/- 0.1V threshold, nominal range 0V to 2.5V, high impedance, DC coupled with an approximately 10 kOhm pull down in standard configuration. Can be hardware configured for different threshold voltages from 0.15 to 2.35V, as AC or DC coupled with or without a termination. The standard hardware configuration connects this to a 4X4 non-blocking cross-point switch allowing multiple uses as a clock or trigger routed to the FMC-1000 PLL and the carrier. When connected to the PLL input (SYNCIn0/CLKin0) it can also be used for cyclical sync or clock signals. This pin can be hardware configured for bidirectional connection to the FMC carrier interface (2.5V LVCMOS). Also this input can be hardware configured for direct PLL “single shot” sync signals (PLL SYNC PIN 6 supports basic “single shot” sync in addition to higher level PLL modes, like triggering a controlled number of SYSREF pulses). PLL pin 6 should not be used for cyclical signals as it can AC crosstalk to the PLL outputs (instead use SYNCIn0/CLKin0 for cyclical signals)
TRIG IO	J6	Hardware Configurable IO, Standard configuration; sampling clock monitor output 0.4V to 1.65 Vpp into 50 Ohms, with weak DC bias from Vref (1V nominal) see block diagram for possible hardware configurations
D/A 0	J2	D/A analog output 50 Ohm nominal impedance AC or DC coupled by model
D/A 1	J3	D/A analog output 50 Ohm nominal impedance AC or DC coupled by model
ALL	ALL	*ENTERTEC 13460334 SSMC JACK RIGHT ANGLE EXTENDED BARREL*

Note: 2.5 V logic inputs absolute maximum 2.8V, absolute minimum -0.3V

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Operating Environment Ratings

Modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		L0	L1	L2	L3	L4
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

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Standard Features

Analog Inputs	
Inputs	2
Input Type	Single ended; AC or DC coupled
Nominal Input Impedance	50 ohm
A/D Device	Analog Devices AD9680BCPZ-1250
Resolution	14-bit
f_{ADC}* Sample Rate	300 MHz to 1250 Msps (each input, A/D IC data transfer rate is 2X)
Aperture Jitter	55 fs

Analog Outputs	
Outputs	2
Output Type	Single ended; AC or DC coupled
Nominal Output Impedance	50 ohm
D/A Device	Texas Instruments DAC38J82
Resolution	16-bit
f_{DAC}* Update Rate	100 to 1230 Msps (1x interpolation) 100 to 2460 Msps (2x interpolation) 100 to 2500 Msps (>=4x interpolation) (each output, D/A IC data transfer rate is 2X)
Interpolation	1x to 16x (11 clock cycle digital latency possible with no interpolation (1x), FIFO off, mixer off, QNC off, and inverse sinc off)

Clocks and Triggering	
Clock Sources*	LMK04828 dual loop PLL 1st loop 100 MHz TCVCXO standard 2nd loop 2 VCOs on chip VCO0 from 2370 to 2630 MHz VCO1 from 2920 to 3080 MHz 1000 MHz Jitter (VCO2 at 3GHz with Output Divider = 3 (1-32 allowed)) < 100 fs (10 kHz to 20 MHz) < 140 fs (100 Hz to 150 MHz)
	External (user supplied)
PLL Reference	External or 25MHz TCXO 25MHz ref is +/-250ppb -40to +85C (used for FMC-1000 test and specification)
PLL Resolution*	<12 kHz typical tuning resolution (depends on PLL configuration)
Triggering	Software: Continuous or acquire N frames External: DC coupled Logic Input
Channel Clocking	All channels can be synchronized to (TBD) clock cycles
Multi-card Synchronization	External triggering and clock inputs may be used for synchronization, and sync signals can be set through the FMC PLL SPI control interface.

*Possible clock and sample rates in an application can depend on hardware configuration, carrier and system design

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Analog Channels Crosstalk	Adjacent Channel	< -70	dB	Measured on terminated victim channel, other 95% FS 70.1 MHz sine
	A/D to/from D/A	< -90	dB	Measured on terminated victim channel, other 95% FS 70.1 MHz sine

FMC Interface	
IO	LA[33:0] pairs, HA[23:0] pairs & HB[21:0] pairs (un-driven pins grounded for improved signal integrity) DP[0..7]_C2M_N,P (JESD 204B subclass 1 DAC data lanes up to 12.5 Gbps each*) DP[0..3]_M2C_N,P (JESD 204B subclass 1 ADC data lanes up to 12.5 Gbps each*)
IO Standards	FMC DP: JESD204B (subclass 1) FMC LA, HA and HB: Differential: LVDS Single Ended: 2.5V LVCMOS FMC Control Signals: 3.3V LVTTL FMC Clocks (bidirectional clocks driven by carrier): LVDS
Required voltages	FMC 3P3V and 3P3VAUX = 3.3V +/- 4% FMC VADJ = 2.5V +/- 4% In order to reduce FMC-1000 power consumption, FMC Voltages are used without re-regulation and are specified at +/-4% (this is not usually a problem as FMC-1000 maximum supply currents are smaller than the FMC maximums where worse case supply voltage droop usually occurs), the FMC-1000 can function with wider Voltage tolerance but is specified with +/-4% Voltage supplies. FMC 12P0V (12V) is not used in standard FMC-1000 hardware configurations, it is routed to a wire terminal / test point on the FMC-1000 for optional system / customer use.

*Possible rates in an application can depend on hardware configuration, carrier and system design

Power		
All AC coupled	Total	10.4W
	3.3V	6.9W (2.1A)
	2.5V Vadj	3.5W (1.4A)
All DC coupled	Total	12W
	3.3V	8.2W (2.5A)
	2.5V Vadj	3.8W (1.52A)
Heat Sinking		Conduction cooling supported, system level thermal design may be required

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A/D ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter		Typ	Units	Notes
A/D Channels				
Bandwidth		10, 1000	MHz	-3dB, AC coupled inputs
		1000	MHz	-3dB, DC coupled inputs
Flatness		+/-0.4	dB	50 to 500 MHz, AC Coupled
		+/-0.5	dB	0 to 500 MHz, DC Coupled
Range	AC Coupled	2	Vpp	Nominal
		10	dBm	Nominal in a 50 Ohm system
		2.6	Vpp	Absolute maximumz
		+/-10	V	DC withstanding from 0V
	DC Coupled	+/-0.42	V	Nominal from 0V
		2.5	dBm	Nominal in a 50 Ohm system
		+/-1	V	Absolute maximum from 0V
SNR		66.2, 61	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		65.8, 60	dB	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		64.9, 59	dB	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
ENOB		10.8, 9.9	bits	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC, DC Coupled
		10.7, 9.5	bits	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		10.5, 8.7	bits	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
SFDR		83, 78	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		80, 55	dB	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		78, 50	dB	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
THD		-83, -79	dBc	Fin = 70.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		-79, -57	dBc	Fin = 141.1 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
		-77, -52	dBc	Fin = 252.85 MHz, 95% FS, sine sampled at 1000 MSPS; AC,DC Coupled
NSD		-153.8, -150.3	dBFS/Hz	F = 70.1 MHz; AC,DC Coupled
		-153.2, -150.1	dBFS/Hz	F = 141.1 MHz; AC,DC Coupled
		-151.9, -149.5	dBFS/Hz	F = 252.85 MHz; AC,DC Coupled
Offset Error (absolute value maximum)		1	mV	Factory calibration, average of 64K samples after warmup.
Gain Error (absolute value maximum)		0.5	%	Factory calibration after warmup.

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D/A ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, f_{DAC} =2 Gsps, 95%FS, 2X interpolation,PLL enabled unless otherwise noted.

Parameter		Typical	Units	Notes
DAC Channels				
Bandwidth**		10, 1000	MHz	Typical, AC Coupled
		600	MHz	Typical, DC Coupled
Output Amplitude Variation**		+/-0.4	dB	10-500 MHz, AC Coupled
		+/-0.5	dB	0-300 MHz, DC Coupled (from a best fit line with gain slope of approximately 0.4dB/100MHz)
Range	AC Coupled	0.9	Vpp	Nominal
		2	dBm	Nominal in a 50 Ohm system
		+/-10	V	DC withstanding from 0V
	DC Coupled	+/- 0.5	V	Nominal from 0V
		2.5	dBm	Nominal in a 50 Ohm system
SNR***		72.5, 68	dB	Fout = 70.1 MHz, 95% FS sine; AC,DC Coupled
		70, TBD	dB	Fout = 141.1 MHz, 95% FS sine; AC,DC Coupled
		64, TBD	dB	Fout = 252.85 MHz, 95% FS sine; AC,DC Coupled
SFDR***		77, 55	dB	Fout = 70.1 MHz, 95% FS sine; AC,DC Coupled
		71, TBD	dB	Fout = 141.1 MHz, 95% FS sine; AC,DC Coupled
		66, TBD	dB	Fout = 252.85 MHz, 95% FS sine; AC,DC Coupled
THD***		-73, -55	dBc	Fout = 70.1 MHz, 95% FS sine; AC,DC Coupled
		-70, -TBD	dBc	Fout = 141.1 MHz, 95% FS sine; AC,DC Coupled
		-65, -TBD	dBc	Fout = 252.85 MHz, 95% FS sine; AC,DC Coupled
NSD***		-160.5, -155	dBFS/Hz	F = 70.1 MHz; AC,DC Coupled
		-158.6, TBD	dBFS/Hz	F = 141.1 MHz; AC,DC Coupled
		-155.5, TBD	dBFS/Hz	F = 252.85 MHz; AC,DC Coupled
Gain Error (absolute value maximum)		0.5	% of FS	Calibrated
Offset Error (absolute value maximum)		1	mV	Calibrated

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Notes:

** Bandwidth and flatness are specified from the DAC IC pin/bump to the FMC-1000 output connector. DAC bandwidth and flatness are application, signal processing and signal dependent. For example assuming 1000 Msps base-band operation the Sync (sin(x)/x) roll off intrinsic to D/A conversion would reduce the amplitude by approximately -6dB at 300 MHz. However the DAC IC has a 9 tap inverse sinc filter capability which could effectively remove this Sinc function from the IC output to above 400 MHz. However this would likely require an aggressive image rejection filter on the output to pass 400 MHz with low loss and attenuate the undesired image starting at 500 MHz, which would likely impact system BW and flatness.

***FMC-1000 analog performance is specified like the D/A IC is specified with a 20 mA full scale output. The FMC-1000 maximum output range is specified at, and the hardware is configured for approximately 30 mA full scale, the maximum full scale amplitude of the D/A IC. The D/A full scale output current can be set in 1/16 increments of the maximum using the D/A IC's 4 bit coarse gain control. This allows a setting of 20.625 mA which is less than 3.2% larger than 20 mA. This difference (0.26dB) is not significant for analog specification purposes. However the output range will be scaled proportionally (11/16) when this is done.

500 MHz BW was used for DAC SNR.

Gain Definition

FMC-1000 is specified and tested with a 50 Ohm source impedance (unless otherwise noted). The FMC-1000 nominal gain is approximately 1X or 0dB when calibrated, the voltage at the FMC-1000 input equals the digital reading output. The internal hardware (raw) gain of the FMC-1000 may be different, for example when DC coupled the A/D IC sees about twice the voltage applied at the FMC-1000 input.

Variations in source impedance change the system gain. The 50 Ohm terminations in a RF system are rarely physical resistors (they are the Thévenin equivalent of the circuit). At lower input frequencies 50 Ohm source terminations are not common but are needed for continuity with higher frequency 50 Ohm measurements. This source 50 Ohm series termination forms a voltage divider with the FMC-1000 input impedance reducing the source voltage by approximately ½ at the FMC-1000 input. Replacing it with a series 0 Ohm source resistance will change the system gain about 2X in Voltage or 6 dB.

Digital Calibration Note

The FMC-310 can be digitally calibrated for offset and gain. However if the signal is clipped (outside the A/D range) the information is lost, so the raw gain is typically designed for a signal level at the A/D that is slightly less than A/D Full Scale in the bandwidth of interest to allow the nominal input range to be measured accurately without clipping when digitally calibrated.

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