FMC-310

V1.6 5/6/14

FMC Module with 4x 310 MSPS 16-bit A/D with PLL and Timing Controls

FEATURES

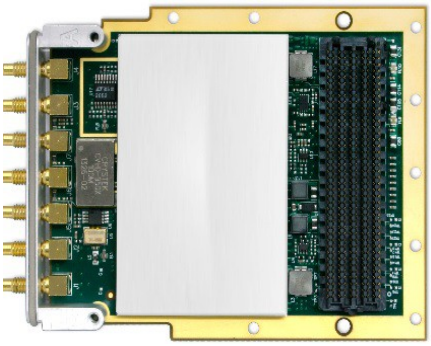
- Four A/D Inputs
  - 310 MSPS, 16-bit
  - AC or DC coupled
- Sample clocks and timing and controls
  - Both Front panel and FMC Ref Clock and Trig/Sync inputs
  - Front panel Clock/Vref output
  - Programmable PLL
  - 20 MHz TCVCXO Ref
- FMC module, VITA 57.1
  - High Pin Count
    - No SERDES required
    - 2.5V VADJ
  - Power monitor and controls
- <10W typical (AC-coupled inputs)
- Conduction Cooling Supported
- Environmental ratings for -40 to 85C 9g RMS sine, 0.1g2/Hz random vibration

APPLICATIONS

- Wireless Receiver
- LTE, WiMAX Physical Layer
- RADAR
- Medical Imaging
- High Speed Data Recording

SOFTWARE

- MATLAB/VHDL FrameWork Logic



DESCRIPTION

The FMC-310 is a high speed digitizing FMC module featuring four 310 MSPS A/D channels supported by sample clock and triggering features. Analog inputs may be either AC or DC coupled. Receiver IF frequencies of up to 300 MHz are supported in the standard model. The sample clock is from either an ultra-low-jitter PLL or external input. Multiple cards can be synchronized for sampling.

The FMC-310 power consumption is 10.1W for typical AC coupled operation (< 12.1W typ. DC). The module may be conduction cooled using provided interfaces, which, while electrically isolated from circuit ground consistent with the FMC standard, are well inter-connected to thermal interfaces on both sides of the FMC-310 providing better and more thermal interfaces. Also the analog shields (large white rectangle, and much smaller adjacent silver rectangular VCXO component shield in the image) are connected to circuit ground, and so are directly thermally connected to the FMC-310 circuits, and can be used for heat management. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

Support logic in VHDL is provided for integration with FPGA carrier cards. Specific support for Innovative carrier cards includes integration with Framework Logic tools that support VHDL/Verilog and Matlab developers. The Matlab BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator for the FMC integrated with the FPGA carrier card.

Software tools for Innovative carrier cards include host development include C++ libraries and drivers for Windows and Linux. Application examples demonstrating the module features are provided.

FMC-310

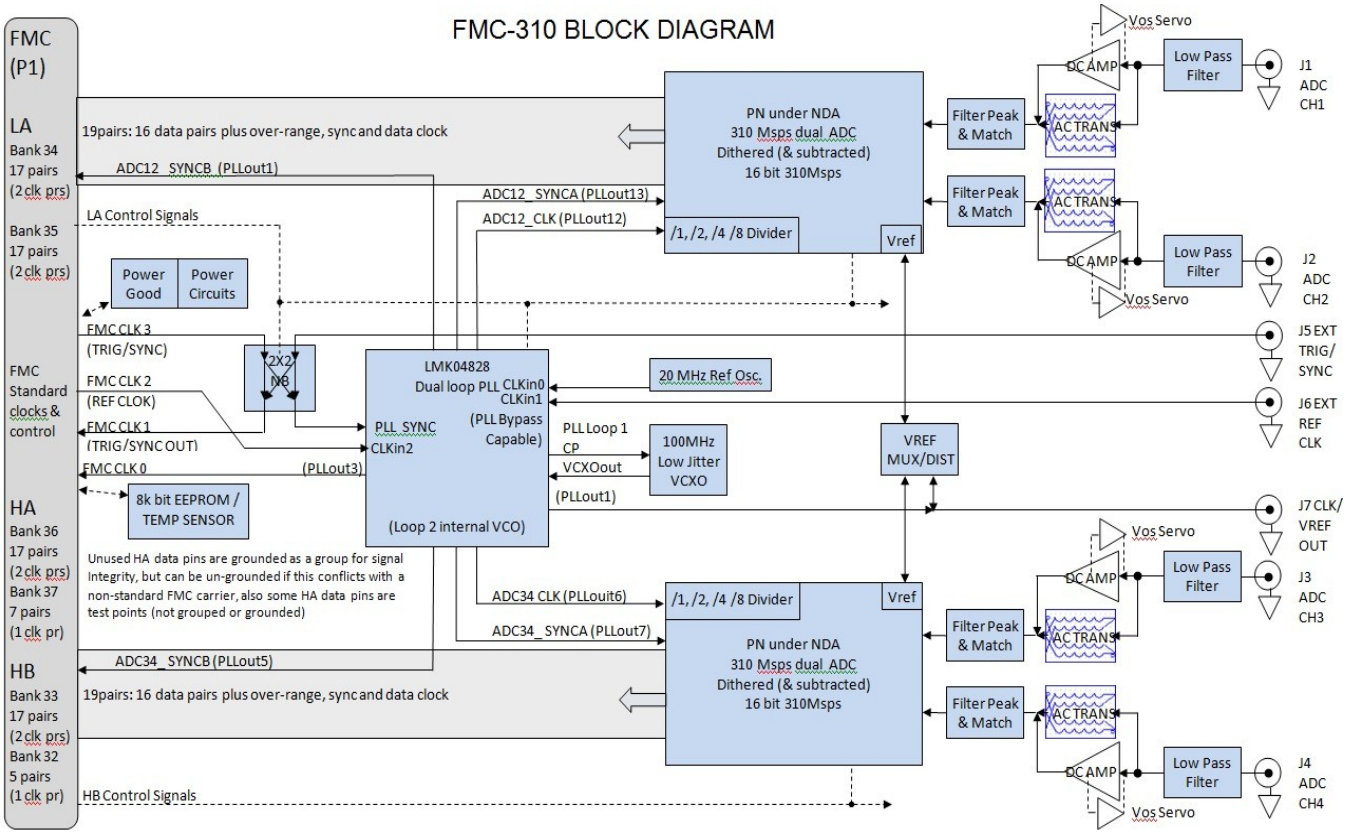
This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

Product	Part No.	Description
FMC-310	80320-1-<ER>	FMC module with four 310 MSPS 16-bit A/Ds, PLL and timing controls, AC- coupled ADCs
FMC-310	80320-2-<ER>	Like 80320-1 except ADCs are DC-coupled
Cables		
SSMC to BNC cable	67156	IO cable with SSMC (male) to BNC (male), 1 meter
Carrier Cards		
PEX6-COP	80284	Desktop/server PCI Express FPGA co-processor card with FMC site
SBC-K7	90326	Single board computer with Kintex 7 FPGA, COM Express
Embedded Computer Hosts		
ePC-K7	90502	ePC-K7, I7 CPU, K325T2 Commercial FPGA. Embedded PC with support for two FMC modules; COM Express Type 6 CPU; Windows/Linux drivers
Mini-K7	90600	Mini-K7, I7 CPU, K325T2 Commercial FPGA. Embedded PC with support for one FMC modules; COM Express Type 6 CPU; Windows/Linux drivers

Physicals	
Form Factor	FMC VITA 57.1 single-width
Size	94.2 mm [front of assembly (RF connectors) to back of assembly (printed circuit board)] x 69 mm 10 mm mounting height
Weight	150g
Hazardous Materials	Lead-free and RoHS compliant

FMC-310


FMC-310 BLOCK DIAGRAM
FMC (P1)
LA
Bank 34
17 pairs
(2 clk prs)
Bank 35
17 pairs
(2 clk prs)
FMC Standard clocks & control
HA
Bank 36
17 pairs
(2 clk prs)
Bank 37
7 pairs
(1 clk pr)
HB
Bank 33
17 pairs
(2 clk prs)
Bank 32
5 pairs
(1 clk pr)
19pairs: 16 data pairs plus over-range, sync and data clock
ADC12_SYNCB (PLLout1)
LA Control Signals
Power Good
Power Circuits
FMC CLK 3 (TRIG/SYNC)
FMC CLK 2 (REF CLOK)
FMC CLK 1 (TRIG/SYNC OUT)
FMC CLK 0
(PLLout3)
2X2 NB
8k bit EEPROM / TEMP SENSOR
Unused HA data pins are grounded as a group for signal Integrity, but can be un-grounded if this conflicts with a non-standard FMC carrier, also some HA data pins are test points (not grouped or grounded)
ADC34_SYNCB (PLLout5)
19pairs: 16 data pairs plus over-range, sync and data clock
HB Control Signals
LMK04828
Dual loop PLL
PLL_SYNC
CLKin2
CLKin0
CLKin1
(PLL Bypass Capable)
(Loop 2 internal VCO)
20 MHz Ref Osc.
PLL Loop 1
CP
VCXOout
(PLLout1)
100MHz Low Jitter VCXO
VREF MUX/DIST
ADC12_SYNCA (PLLout13)
ADC12_CLK (PLLout12)
/1, /2, /4 /8 Divider
Vref
PN under NDA
310 Msps dual ADC
Dithered (& subtracted)
16 bit 310Msps
ADC34 CLK (PLLouit6)
ADC34_SYNCA (PLLout7)
/1, /2, /4 /8 Divider
Vref
PN under NDA
310 Msps dual ADC
Dithered (& subtracted)
16 bit 310Msps
Filter Peak & Match
Filter Peak & Match
Filter Peak & Match
Filter Peak & Match
AC TRANS
AC TRANS
AC TRANS
AC TRANS
Vos Servo
DC AMP
Low Pass Filter
J1 ADC CH1
Vos Servo
DC AMP
Low Pass Filter
J2 ADC CH2
J5 EXT TRIG/ SYNC
J6 EXT REF CLK
Vos Servo
DC AMP
Low Pass Filter
J7 CLK/ VREF OUT
J3 ADC CH3
Vos Servo
DC AMP
Low Pass Filter
J4 ADC CH4

FMC-310

Block Diagram Optional Feature Notes:

Optional Vos Servo Circuit:

The standard DC coupled FMC-310 employs digital calibration to remove input offset (Vos) which is the best choice for most applications. The superior analog performance of the DC coupled FMC-310 results from the use of a high performance differential input balanced amplifier. One amplifier input is used and the other is internally terminated to ground with a 50 Ohm resistor. But if there is a DC (or very low frequency) input applied to the FMC-310 input, the differential amplifier will see a DC bias or imbalance, typically reducing analog performance. The optional Vos servo converts an applied DC or low frequency input to differential at the amplifier inputs restoring the DC balance and bias point. This is also useful for reducing the FMC-310 hardware input offset, and accommodating non-50 Ohm inputs.

A trade off when using the optional FMC-310 Vos servo is it changes the DC coupled FMC-310 input impedance from 50 Ohms at low frequencies (below 200 Hz), down to approximately 15 Ohms at DC, introduces up to +/-8% variation in the 50 Ohm input impedance between 200Hz and 120kHz, but is well matched to 50 Ohms above 120 kHz to the upper operating frequency limit. The servoed DC coupled FMC-310 will accurately measure a 50 Ohm series terminated input voltage down to DC, but the connected circuit will “see” the FMC-310 input impedance change at low frequencies.

Optional Voltage Reference Multiplexor/Distribution and J7 Clock/Vref Connector:

The standard configuration buffers the voltage reference from the ADC used for channels 1 and 2 to provide a DC level at J7, allowing this to be used as a test point to verify the ADC's Vref setting. The optionally hardware configured Vref MUX/DIST circuit allows for either ADCs' voltage reference, or an external Voltage reference applied to J7, to be scaled and source the other ADC's reference voltage or buffered to source J7's DC Voltage. Allowance is also made for using an internal low noise 1.8V supply as a reference. J7's circuit is configured as a bias tee allowing an AC coupled PLL output (could be sample clock, reference, sync or other PLL generated frequency) to be combined with this DC level.

Optional Low Pass Filters on Inputs:

On standard product these are populated with 1200 MHz (-1dB BW) low pass filters intended to filter high frequency EMI while not impacting signal bandwidth. Lower frequency options are possible. Also can be used in conjunction with...

Optional Filter, Peak and Match circuits at ADC Inputs:

A low pass filter and a bandpass filter are allowed for at the ADC input. These are designed to incorporate the ADC parasitic circuit in the filters, and reduce the broadband noise bandwidth at the ADC input.

Minimum lot sizes, set-up, stocking and NRE charges may apply. Contact sales support for pricing and availability.

FMC-310

Operating Environment Ratings

Modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance. System compliance can depend on application, and system.

Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

FMC-310

Standard Features

Analog Input	
Inputs	4 Standard Product Inputs Analog performance is specified with a +/-0.5 Vp, 1 Vpp, approx. 4 dBm pure sine (with ADC set to Vref = 1.0V, 2Vpp FS) A 1 Vpp sine input in the middle pass band frequencies corresponds to approx. 1.9 Vpp at the ADC IC (both AC and DC coupled) The standard FMC-310 is digitally corrected for full scale, gain and offset at the input connector (single point calibration)
Input Range	+/-0.5 Vp, 1 Vpp (approx. 4 dBm sine) full scale (adjustable from approximately 0.625 to 1.25 Vpp digitally, in steps, using on-board voltage reference circuits)
Input Type	Single ended; AC or DC coupled
Nom. Input Impedance	50 ohm
A/D Device	Analog Devices AD9652Under NDA (16-bit dual ADC)
A/D Jitter	40 fs Aperature
A/D Sample Rate	80 Msps to 310 Msps (Maximum 1240 MHz applied clock, ADC IC can divide by 1,2,4 or 8)

Clocks and Triggering	
Clock Sources	LMK04828 dual loop PLL 1st loop 100 MHz TCVCXO standard 2nd loop 2 VCOs on chip VCO0 from 2370 to 2630 MHz VCO1 from 2920 to 3080 MHz 300 MHz Jitter (VCO2 at 3GHz with Output Divider = 10 (1-32 allowed)) < 100 fs (10 kHz to 20 MHz) < 140 fs (100 Hz to 150 MHz)
	External (user supplied)
PLL Reference	External or 20MHz TCXO option 20MHz ref is +/-250ppb -40to +85C (used for FMC-310 specification)
PLL Resolution	<12 kHz Typical Tuning Resolution (depends on PLL configuration)
Triggering	External, software, acquire N frames
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels can be synchronous
Multi-card Synchronization	External triggering and clock inputs may be used for synchronization, and sync signals can be set through the FMC PLL SPI control interface.

FMC Interface	
IO	LA[33:0] pairs, HA[23:0] pairs, HB[21:0] pairs
IO Standards	LA, HA and HB: Differential: LVDS Single Ended: 2.5V LVCMOS
Required FMC carrier supplied voltages	3.3V (2.2A Max.) 3.3V AUX (10 mA Max.) VADJ = 2.5V (3.35A Max.: 2.20A Max. used on FMC-310, 1.15A Max. to FMC VIO_B_M2C

Power	
Consumption	10.1W all channels AC Coupled 12.1W all channels DC coupled Maximums based on recommended / expected usage.
Heat Sinking	Conduction cooling supported (does not include thermal interface near FMC region 1 RF connectors)

FMC-310

ELECTRICAL CHARACTERISTICS

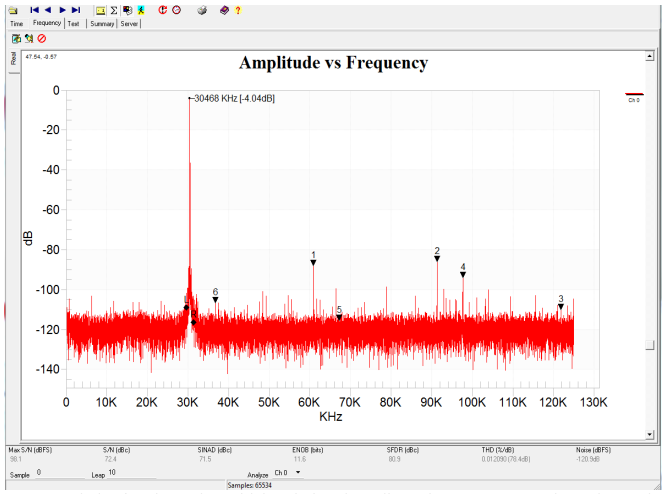
Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
A/D Channels			
Analog Input Bandwidth	300	MHz	-3dB, DC coupled inputs
	0.5 to 300	MHz	-3dB, AC coupled inputs
Analog Input Passband Flatness	+/-0.4	dB	0 to 155 MHz, DC Coupled
	+/-0.4	dB	10 to 155 MHz, AC Coupled
Broadband SFDR	80, 79	dB	Fin = 5.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
	82, 80	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
Harmonic Distortion	-81, -79	dB	Fin = 5.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
	-83, -81	dB	Fin =70.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
ENOB	11.6, 10.5	bits	Fin = 5.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
	11.5, 10.3	bits	Fin = 70.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
SNR	71, 64	dB	Fin = 5.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
	70, 63	dB	Fin = 70.1 MHz, 95% FS, sine sampled at 300 MSPS; (AC, DC) Coupled
Crosstalk	< -90	dB	Measured channel grounded with a 70.1 MHz, 95% FS sine input on adjacent channel (channels 1,2 to/from channels 3,4 are better isolated)
Offset Error	+/- 1	mV	With digital calibration, average of 64K samples after warm up. Worst case uncalibrated hardware offset error is +/- 25mV Optional DC Coupled Vos servo uncalibrated hardware offset error is +/- 1mV typical (+/-7mV worst case) after warm-up which may also be effectively reduced with digital calibration
Gain Error	<0.5	%	Factory calibration after warmup.

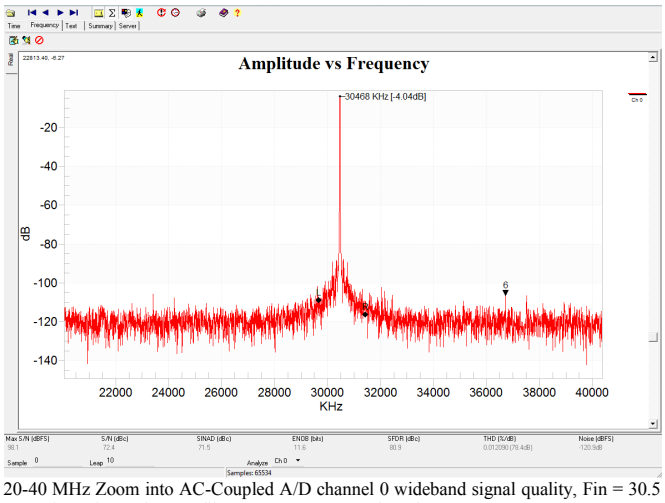
FMC-310

ELECTRICAL CHARACTERISTICS

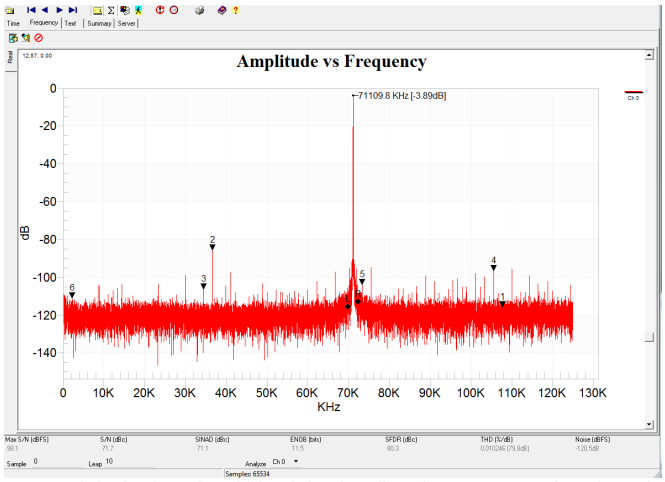
Measurements taken with a prototype, better performance is projected in the production design....



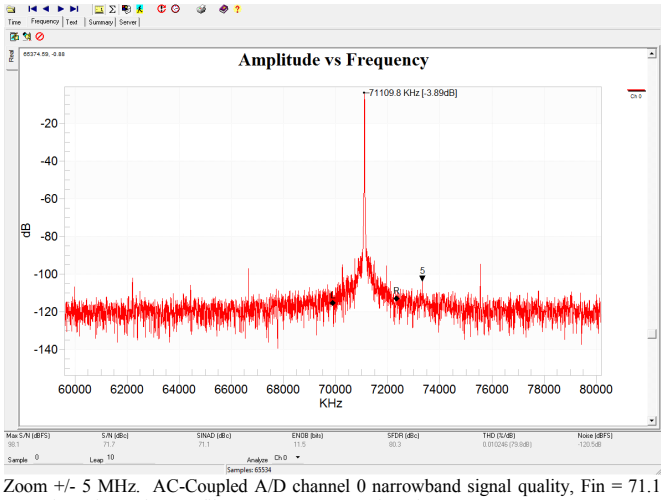
AC-Coupled A/D channel 1 wideband signal quality, Fin = 30.5 MHz through 7-pole TTE filter, Fs = 310 MHz onboard PLL.



20-40 MHz Zoom into AC-Coupled A/D channel 0 wideband signal quality, Fin = 30.5 MHz through 7-pole TTE filter, Fs = 310 MHz onboard PLL.

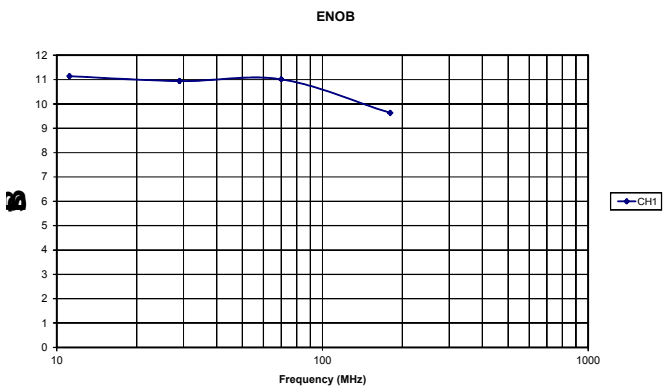


AC-Coupled A/D channel 0 wideband signal quality, Fin = 71.10 MHz through 7-pole TTE filter, Fs = 310 MHz onboard PLL.

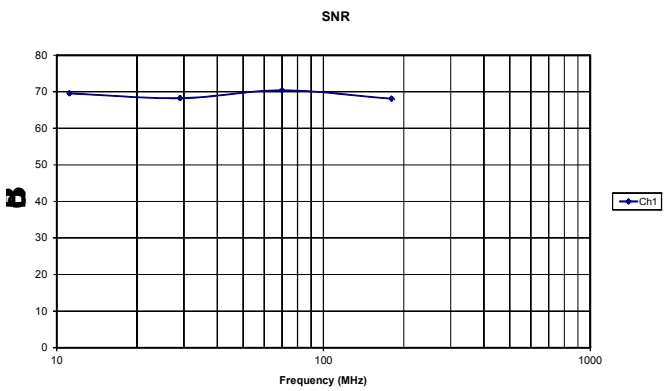


Zoom +/- 5 MHz. AC-Coupled A/D channel 0 narrowband signal quality, Fin = 71.1 MHz through 7-pole TTE filter, Fs = 310 MHz onboard PLL.

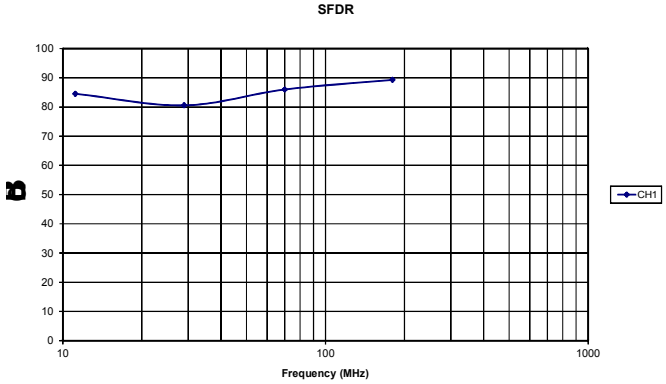
FMC-310



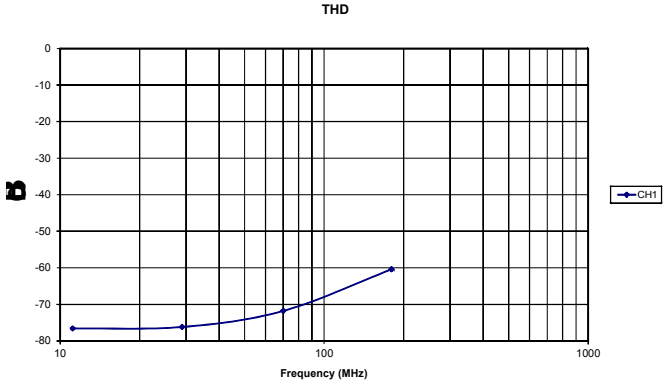
DC-Coupled A/D ENOB vs Frequency. Fs = 310 MHz onboard PLL.



DC-Coupled A/D SNR vs Frequency. Fs = 310 MHz onboard PLL.



DC-Coupled A/D SFDR vs Frequency. Fs = 310 MHz onboard PLL.



DC-Coupled A/D THD vs Frequency. Fs = 310 MHz onboard PLL

DC-Coupled A/D Frequency Response. Fs = 310 MHz onboard PLL.

FMC-310

IMPORTANT NOTICES

Innovative Integration Incorporated reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Innovative Integration's terms and conditions of sale supplied at the time of order acknowledgment.

Innovative Integration warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with Innovative Integration's standard warranty. Testing and other quality control techniques are used to the extent Innovative Integration deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Innovative Integration assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using Innovative Integration products. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Innovative Integration does not warrant or represent that any license, either express or implied, is granted under any Innovative Integration patent right, copyright, mask work right, or other Innovative Integration intellectual property right relating to any combination, machine, or process in which Innovative Integration products or services are used. Information published by Innovative Integration regarding third-party products or services does not constitute a license from Innovative Integration to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Innovative Integration under the patents or other intellectual property of Innovative Integration.

Reproduction of information in Innovative Integration data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice.

Innovative Integration is not responsible or liable for such altered documentation. Resale of Innovative Integration products or services with statements different from or beyond the parameters stated by Innovative Integration for that product or service voids all express and any implied warranties for the associated Innovative Integration product or service and is an unfair and deceptive business practice. Innovative Integration is not responsible or liable for any such statements.