InnoDisk FiD2.5” ATA8000-J

Datasheet

Rev. 1.0

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REVISION HISTORY

Revision	Description	Date
Preliminary	First Released	2009/03/05
0.1	1. Modify theory of operation, including SATA II controller and host bridge description. 2. Correct electrical connections 3. Remove hot plug support	2009/03/31
0.2	1. Add access time value 2. Add mechanical dimensions value	2009/6/17
0.3	1. Modify power requirement	2009/6/30
1.0	1. Remove transfer timing part 2. Wording correction 3. Update product performance and UDMA info.	2009/9/11

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1. Product Overview

1.1 Introduction of InnoDisk FiD 2.5” ATA 8000-J

InnoDisk FiD 2.5” ATA8000-J provide high capacity 2.5-inch solid-state flash disk that electrically complies with ATA 7 standard, and supports Ultra DMA (0-6) and PIO (0-4) transfer modes.

Regarding performance of InnoRobust PATA SSD, sustained read is 87 MB per second (max.), and sustained write is 80 MB per second (max).

InnoDisk FiD 2.5” ATA8000-J is designed for industrial field. The SSD have good performance, no latency time and small seek time. It effectively reduces the booting time of operation system and the power consumption is less than hard disk drive (HDD). InnoDisk FiD 2.5” ATA8000-J can work in harsh environment. It is vibration resistance, and can work in lower or higher temperature than HDD. InnoDisk FiD 2.5” ATA8000-J complies with ATA protocol, no additional drives are required, and the SSD can be configured as a boot device or data storage device.

1.2 Product View

Figure 1 InnoDisk FiD 2.5” ATA 8000-J

1.3 Product Models

InnoDisk FiD 2.5” ATA 8000-J is available in following capacities.

FiD 2.5” ATA8000-J 8GB FiD 2.5” ATA8000-J 16GB

FiD 2.5” ATA8000-J 32GB FiD 2.5” ATA8000-J 64GB

FiD 2.5” ATA8000-J 128GB

2. Theory of operation

2.1 Overview

Figure 2 shows the operation of InnoDisk FiD 2.5" ATA 8000-J from the system level, including the major hardware blocks.

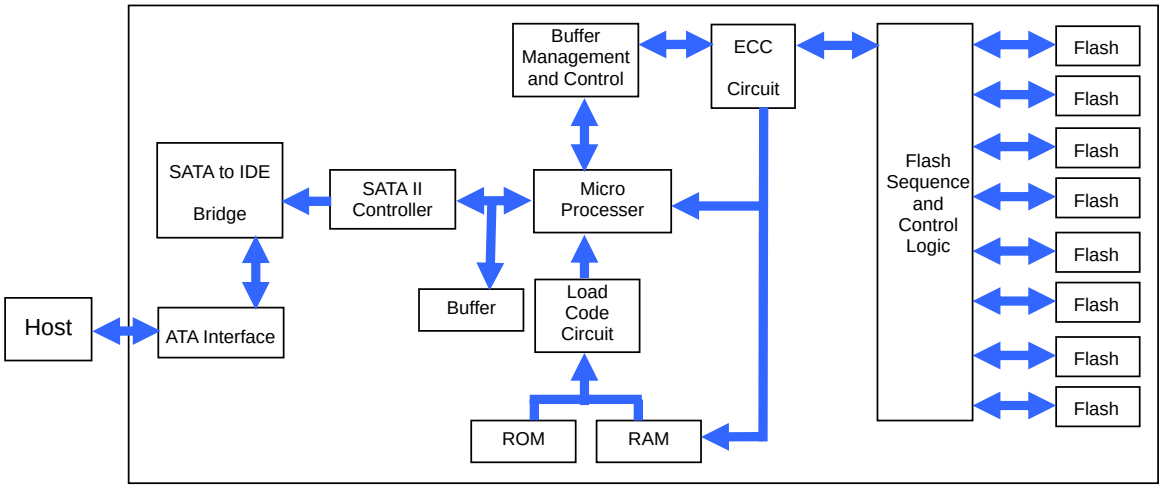

Figure 2 InnoDisk FiD 2.5" ATA 8000-J Block Diagram

InnoDisk FiD 2.5" ATA 8000-J integrates a SATA to IDE Bridge, SATA II controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 SATA II Controller

This SATA II controller is designed within independent 8 channels for flash interface and which is equipped with 96KB of internal memory. 64 KB of memory is used for data buffer, and 32 KB is used for general purpose. The internal memory can also be used as an intermediate memory for storing data blocks during a wear-leveling procedure. There are 40KB of internal memory is used for code. A 10KB internal boot ROM includes basic routines for accessing the flash memories and for loading the main code into the internal memory.

2.3 Host Bridge

The host bridge plays a converter role between the SATA II controller and host IATA protocol. It accepts Parallel ATA (IDE) commands through the 44pin IDE connector physically from the host and decodes the commands and then converts them to SATA commands to the SATA II controller whose responses through the SATA bus are deciphered, processed and converted to the ATA protocol and sent to the host.

2.4 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 8 bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.5 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the *erase cycle limit* or *write endurance limit* and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

InnoDisk FiD 2.5” ATA 8000-J uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

2.6 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. The Bad Blocks will not exceed more than 6.7% of the total device volume. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

3. Installation Requirements

3.1 Pin Assignments

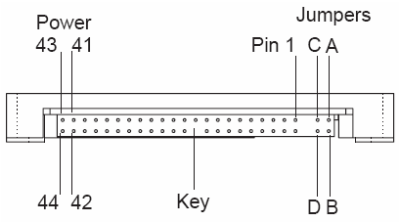

Figure 3 FiD 2.5” ATA8000-J Connector Layout

3.2 Electrical Connections for FiD 2.5 ATA 8000-J

FiD 2.5” ATA8000-J is design with an IDE 2.00mm pin pitch interface connector and thus which can be directly connected to an IDE host or to a female 44pin connector and then to a host. For the connection through a cable, it is suggested that the cable should be no longer than 1meter. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

3.3 Form Factor

Please prepare following things:

- Screw driver.
- Four M3 screws.

4. Specifications

4.1 CE and FCC Compatibility

InnoDisk FiD 2.5” ATA 8000-J conforms to CE and FCC requirements**.**

4.2 RoHS Compliance

InnoDisk FiD 2.5” ATA 8000-J is fully compliant with RoHS directive.

4.3 Environmental Specifications

4.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade：0°C to +70°C
- Industrial Grade：-40°C to +85°C

Storage Temperature Range:

- Standard Grade：-55°C to +95°C
- Industrial Grade：-55°C to +95°C

4.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

4.3.3 Shock and Vibration

Table 1: Shock/Vibration Testing for InnoDisk FiD 2.5” STA 8000-J

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500G, 3 axes	IEC 68-2-27

4.3.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various InnoDisk FiD 2.5” ATA 8000-J configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- Failure Rate: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- Mean Time between Failures (MTBF): A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular

measurement interval under stated conditions.

Table 2: InnoDisk FiD 2.5” ATA 8000-J MTBF

Product	Condition	MTBF (Hours)
InnoDisk FiD 2.5” ATA 8000-J	Telcordia SR-332 GB, 25°C	>3,000,000

4.4 Transfer Mode

InnoDisk FiD 2.5” ATA 8000-J support following transfer mode:

PIO Mode 0~4

Ultra DMA 0~6

4.5 Pin Assignment

InnoDisk FiD 2.5” ATA 8000-J uses a standard ATA pin-out. See Table 3 for InnoDisk FiD 2.5” ATA 8000-J pin assignments.

Table 3: InnoDisk FiD 2.5” ATA 8000-J Pin Assignment

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	KEY	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[1]	Host I/O Write	24	GND	Ground
	STOP[2]	Stop Ultra DMA burst			
25	HIOR[1]	Host I/O Read	26	GND	Ground
	HDMARDY[2]	Ultra DMA ready			
	HSTROBE[2]	Ultra DMA data strobe			
	IORDY[1]	I/O Ready			

27	DDMARDY[2]	Ultra DMA ready	28	CSEL	Master/Slave Select
	DSTROBE[2]	Ultra DMA data strobe			
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41	VCC	Supply Voltage	42	VCC	Supply Voltage
43	GND	Ground	44	NC	Not Connected
A	N/A	Master/Slave	B	N/A	Master/Slave
C	N/A	NC	D	N/A	NC

Note: 1.Signal usage in PIO & Multiword DMA mode.

2.Signal usage in Ultra DMA mode

4.6 Mechanical Dimensions

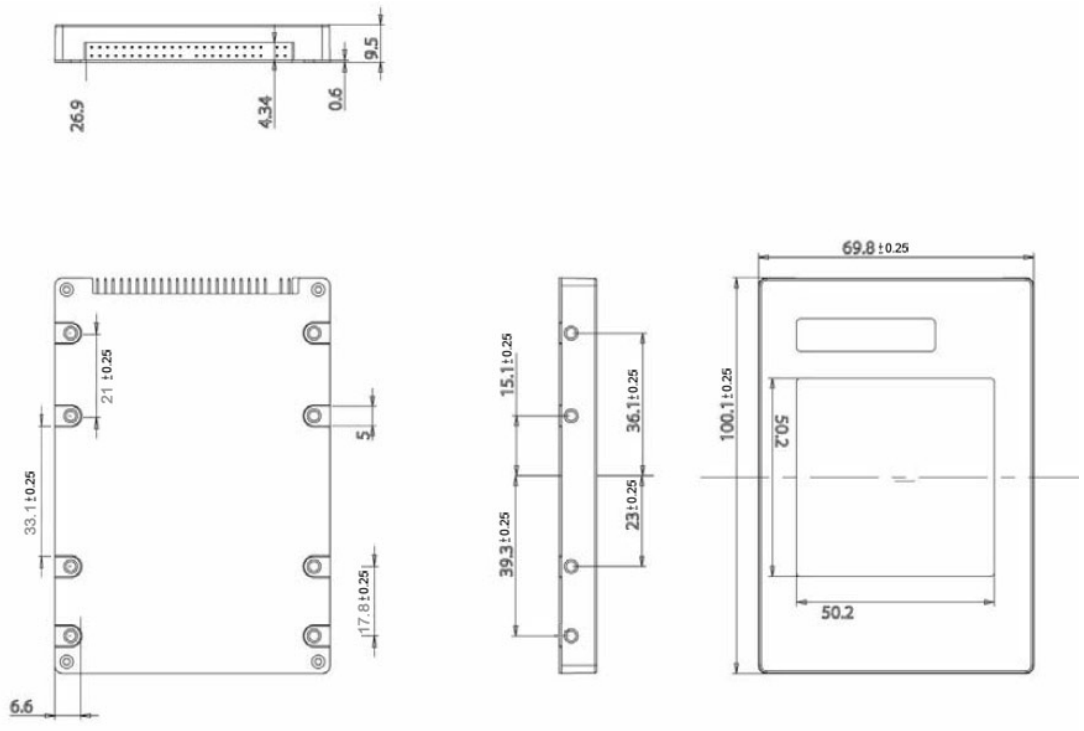

Figure 4 FiD 2.5 ATA 8000-J mechanical dimensions

4.7 Assembly weight

An InnoDisk FiD 2.5" ATA 8000-J within SLC flash ICs, 8GB's weight is 90 grams approx. If the capacity is different, the flash chip's weight needs to be added. However, the total weight of SSD will be less than 95 grams.

4.8 Performance

Sustained Read : 87MB/sec

Sustained Write : 80MB/sec (Base on 32GB)

4.9 Seek Time

InnoDisk FiD 2.5" ATA 8000-J is not a magnetic rotating design. There is no seek or rotational latency required.

4.10 NAND Flash Memory

InnoDisk FiD 2.5" ATA 8000-J uses Single Level Cell (SLC) NAND flash memory, which is non-volatility, high reliability and high speed memory storage. There are only two statuses 0 or 1 of one cell. Read or Write data to flash memory for SSD is control by micro processor.

4.11 Electrical Specifications

4.11.1 Power Requirement

Table 4: InnoDisk FiD 2.5" ATA 8000-J Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+5DC +- 5% 500mA (max.)	V

4.11.2 Power Consumption

Table 5: Power Consumption

Mode	Power Consumption
	SLC
Read	350mA (max.)
Write	400mA (max.)
Idle	200mA (max.)

4.12 Device Parameters

FiD 2.5 ATA 8000-J device parameters are shown in Table 6.

Table 6: Device parameters

Capacity	LBA	Cylinders	Heads	Sectors
8GB	15621984	15498	16	63
16GB	31277056	16383	16	63
32GB	62586880	16383	16	63
64GB	125206528	16383	16	63
128GB	252411904	16383	16	63

5. Supported ATA Commands

5.1 Supported ATA Commands

InnoDisk FiD 2.5" ATA 8000-J supports the commands listed in Table 7.

Table 7: ATA Commands

Command Name	Command Code	Support
Check Power Mode	E5H (98H)	Yes
Execute Device Diagnostic	90H	Yes
Format Track	(50H)	Yes
Identify Device	ECH	Yes
Idle	E3H (97H)	Yes
Idle immediate	E1H (95H)	Yes
Initialize Device Parameters	(91H)	Yes
NOP	00H	Yes
Read Buffer	E4H	Yes
Read Long Sector	(22H or 23H)	Yes
Read Multiple	C4H	Yes
Read Sector(s)	20H or 21H	Yes
Read Verify Sector	40H or 41H	Yes
Read DMA	C8H	Yes
Recalibrate	(1XH)	Yes
Seek	70H	Yes
Set Features	EFH	Yes
Set Multiple Mode	C6H	Yes
Set Sleep Mode	E6H (99H)	Yes
Standby	E2H (96H)	Yes
Standby Immediate	E0H (94H)	Yes
Write Buffer	E8H	Yes
Write Multiple	C5H	Yes
Write Sector	30H	Yes
Write DMA	CAH	Yes
Write Verify	(3CH)	Yes
Security Set Password	F1H	Yes
Security Unlock	F2H	Yes
Security Erase Prepare	F3H	Yes
Security Erase Unit	F4H	Yes
Security Freeze Lock	F5H	Yes
Security Disable Password	F6H	Yes

5.1.1 Check Power Mode

5.1.1.1 Command Code

E5h

5.1.1.2 Feature Set

Power Management feature set.

- This command is mandatory for devices.

-This command is mandatory when the Power Management feature set is implemented.

5.1.1.3 Protocol

Non-data command

5.1.1.4 Inputs

Table 8: Check power mode command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E5h							

Device register

DEV shall specify the selected device.

5.1.2 IDENTIFY DEVICE

5.1.2.1 Command Code

ECh

5.1.2.2 Feature Set

General feature set

-Mandatory for all devices.

-Devices implementing the PACKET Command feature set

5.1.2.3 Protocol

PIO data-in

5.1.2.4 Inputs

Table 9: Identify device command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	ECh							

Device register

DEV shall specify the selected device.

5.1.2.5 Outputs

5.1.2.5.1 Normal outputs

Table 10: Identify device command for normal outputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.2.6 Prerequisites

DRDY set to one.

5.1.2.7 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 8 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0. Some parameters are defined as 32-bit values (e.g. words (61:60)). Such fields are transfer using two successive word transfers. The device will first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits(31:16) of the value, shall be transferred on DD(15:0) respectively. Some parameters are defined as a string of ASCII characters.

Table 11: Identify device command parameters

Word	Description	Value
0	General Configuration Bit 15 0=ATA device Bit 14:8 Retired Bit 7:6 Obsolete Bit 5:3 Retired Bit 2 Response incomplete Bit 1 Retired Bit 0 reserved	0040h
1	Number of logical cylinders	XXXXh
2	Specific configuration	37C8h
3	Number of logical heads	16
4-5	Retired	0000h
6	Number of logical sectors per logical track	63
7-9	Retired	0000h
10-19	Serial number (ATA String)	20 ASCII characters
20-21	Retired	0000h
22	Obsolete	003Fh
23-26	Firmware revision(ATA String)	8 ASCII characters
27-46	Model number(ATA String)	40 ASCII characters
47	15-8: 80 7-0: 00h Reserved 01h-FFh: Maximum number of sectors that shall be transferred per DRQ data block on READ/WRITE Multiple commands	8001h
48	Trusted Computing feature set options 15 shall be cleared to zero 14 shall be set to one 13:1 Reserved for the Trusted Computing Group 0 0 = Trusted Computing feature set is not supported	4000h
49	Capabilities 15-14: Reserved for the IDENTIFY PACKET DEVICE command. 13: 1=Standby timer values as specified in this standard are supported 0:Standby timer values shall be managed by the device 12: Reserved for the IDENTIFY PACKET DEVICE	2F00h

	command 11: 1=IORDY supported 0=IORDY may be disabled 10 1: IORDY may be disabled 9 1=LBA supported 8 1=DMA supported. 7-0 Retired	
50	Capabilities 15: Shell be cleared to zero 14: Shall be set to one 13:2 Reserved 1 Obsolete 0 0	4000h
51	Obsolete	0280h
52	Obsolete	0000h
53	15 Free-fall control Sensitivity 00h: Vendor's recommended setting 7:3 Reserved 2: 1=the fields reported in word 88 are valid 1: 1=the fields reported in words (70:64) are valid 0: Obsolete	0007h
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15:9 Reserved 8 0:Multiple sector setting is invalid 7:0 Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE Multi commands	0001h
60-61	Total number of user address sectors(DWord)	XXXXXXXXh
62	Obsolete	0000h
63	Multi-word DMA transfer(Not support)	0007h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA	0078h

	transfer cycle time per word 15-0 Cycle time in nanoseconds	
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-74	Reserved	0000h
75	No DMA QUEUED command supports	0000h
76	Serial ATA Capabilities 15:11 Reserved for Serial ATA 10 1= Supports Phy Event Counters 9 1= Supports receipt of host initiated power management Requests 8 0= No Support native Command Queuing 7:3 Reserved for future SATA signaling speed grades 2 1=Supports SATA Gen2 Signaling Speed (3.0Gb/s) 1 1=Support SATA Gen1 Signaling Speed (1.5Gb/s) 0 Shall be cleared to zero	0606h
77	Reserved for Serial ATA	0000h
78	Serial ATA features supported 15:7 Reserved for Serial ATA 6 0=Device not supports Software Settings Preservation 5 Reserved for Serial ATA 4 0= Device not supports in-order data delivery 3 0= Device not supports initiating power management 2 0= Device not supports DMA Setup auto-activation 1 0= Device not supports non-zero buffer offsets 0 Shall be cleared to zero	0000h
79	Serial ATA feature enabled 15:7 Reserved for Serial ATA 6 0=Software Settings Preservation not enabled 5 0=Reserved for Serial ATA	0000h

	4 0= In-order data delivery not enabled 3 0= Device initiated power management not enabled 2 0= DMA setup auto-activation not enabled 1 0= Non-zero buffer offsets not enabled 0 Shall be cleared to zero	
80-81	ATA Version support (ATA8-ACS)	01FE 0021h
82	Command and feature sets supported 15 0 = Obsolete 14 0 = NOP Command not supported 13 0 = READ BUFFER Command not supported 12 0 = WRITE BUFFER Command not supported 11 0 = Obsolete 10 0 = Host Protected Area Feature Set not supported 9 0 = DEVICE RESET Command not supported 8 0 = SERVICE Interrupt not supported 7 0 = RELEASE Interrupt not supported 6 1 = Look-ahead supported 5 1 = Write Cache supported 4 0 = indicate that the PACKET feature set is not supported 3 1 = mandatory Power Management Feature Set supported 2 0 = Obsolete 1 0 = Security Mode Feature Set not supported 0 1 = SMART Feature Set supported	0069h
83	Command and feature sets supported 15 Shall be cleared to zero 14 Shall be set to one 13 0 = FLUSH CACHE EXT Command not supported 12 1 = mandatory FLUSH CACHE Command supported 11 0 = Device Configuration Overlay feature set not supported 10 0 = 48-Bit Address feature set not supported 9 0 = Automatic Acoustic Management feature set not supported 8 0 = SET MAX security extension not supported	5000h

	7 0 = See Address Offset Reserved Area Boot, INCITS TR27:2001 6 0 = SET FEATURES subcommand not required to spin-up after power-up 5 0 = Power-Up in Standby feature set supported 4 0 = Removable Media Status Notification feature set not supported 3 0 = Advanced Power Management feature set not supported 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED not supported 0 1 = DOWNLOAD MICROCODE Command supported	
84	Command Set/Feature Supported Extension 15 Shall be cleared to zero 14 Shall be set to one 13-6 Reserved 5 0 = General Purpose Logging feature set not supported 4 reserved 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number not supported 1 0 = SMART self-test not supported 0 1 = SMART Error Logging not supported	4000h
85	Command and feature sets supported or enabled 15 0 = Obsolete 14 0 = NOP Command not enabled 13 0 = READ BUFFER Command not enabled 12 0 = WRITE BUFFER Command not enabled 11 Obsolete 10 0 = Host Protected Area feature set not enabled 9 0 = DEVICE RESET Command not enabled 8 0 = SERVICE Interrupt not enabled 7 0 = RELEASE Interrupt not enabled 6 0 = Look-ahead not enabled 5 0 = Write Cache not enabled 4 Shall be cleared to zero to indicate that the	0008

	PACKET Command feature set is not supported. 3 1 = Power Management Feature Set enabled 2 0 = Removable Media feature set not enabled 1 0 = Security Mode Feature Set not enabled 0 0 = SMART Feature Set not enabled	
86	Command set/feature enabled 15-14 0 = Reserved 13 0 = FLUSH CACHE EXT Command not supported 12 1 = FLUSH CACHE Command supported 11 0 = Device Configuration Overlay not supported 10 0 = 48-Bit Address features set not supported 9 0 = Automatic Acoustic Management feature set not enabled 8 0 = SET MAX security extension not enabled by SET MAX SETPASSWORD 7 0 = Reserved 6 0 = SET FEATURES subcommand required to spin-up after power-up not enabled 5 0 = Power-Up in Standby feature set not enabled 4 0 = Obsolete 3 1 = Advanced Power Management feature set enabled 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED Command not supported 0 1 = DOWNLOAD MICROCODE Command supported	5000h
87	Command and feature sets supported or enabled 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 0 = Reserved for Technical Report, INCITS TR-37-2004 11 0 = Reserved for Technical Report, INCITS TR-37-2004	4000h

	10:9 0 = Obsolete 8 0 = 64-Bit World Wide Name not supported 7 0 = WRITE DMA QUEUED FUA EXT Command not supported 6 0 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands not supported 5 0 = General Purpose Logging feature set not supported 4 0 = Obsolete 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number is not valid 1 0 = SMART Self-Test not supported 0 0 = SMART Error-Logging not supported	
88	Ultra DMA modes 15 Reserved 14 0 = Ultra DMA mode 6 is not supported 13 1= Ultra DMA mode 5 is selected 0= Ultra DMA mode 5 is not selected 12 1= Ultra DMA mode 4 is selected 0= Ultra DMA mode 4 is not selected 11 1= Ultra DMA mode 3 is selected 0= Ultra DMA mode 3 is not selected 10 1= Ultra DMA mode 2 is selected 0= Ultra DMA mode 2 is not selected 9 1= Ultra DMA mode 1 is selected 0= Ultra DMA mode 1 is not selected 8 1= Ultra DMA mode 0 is selected 0= Ultra DMA mode 0 is not selected 7 Reserved 6 0= Ultra DMA mode 6 is not supported 5 1= Ultra DMA mode 5 and below are supported 4 1= Ultra DMA mode 4 and below are supported 3 1= Ultra DMA mode 3 and below are supported 2 1= Ultra DMA mode 2 and below are supported 1 1= Ultra DMA mode 1 and below are supported 0 1= Ultra DMA mode 0 is supported	X03Fh
89	Time required for Normal Erase mode SECURITY ERASE UNIT command	0000h

90	Time required for Enhanced erase mode SECURITY ERASE UNIT command	0000h
91	Current advanced power management level value	0000h
92	Master Password Identifier	0000h
93	Hardware reset result	XXXXh
94	Current automatic acoustic management value 15:8 Vendor's recommended acoustic management value. 7:0 Current automatic acoustic management value.	80FEh
95-126	Reserved	0000h
127	Obsolete	0000h
128	Security Status 15:9 Reserved 8 Security level 0 = high, 1 = Maximum 7:6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 0= Security frozen. 2 0 = Security not locked 1 0= Security not enabled 0 0= Security not supported	0000h
129-159	Vendor specific	0000h
160	CFA power mode 1(Not support)	0000h
161-175	Reserved	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15:8 Check Sum 7:0 Signature	XXXXh

5.1.3 IDLE

5.1.3.1 Command Code

E3h

5.1.3.2 Feature Set

Power Management Feature Set.

5.1.3.3 Protocol

Non-Data

5.1.3.4 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall

determine the time period programmed into the Standby timer.

Table 12: Idle command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Timer period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E3h							

Device register-

DEV shall specify the selected device.

Table 13: Idle command sector count register contents information

Sector Count register contents	Corresponding timeout period
0 (00h)	Timeout disabled
1-240 (01h-F0h)	(value*5)s
241-251 (F1h-FBh)	((Value-240)*30)min
252 (FCh)	21min
253 (FDh)	Period between 8 and 12 hrs
254 (FEh)	Reserved
255 (FFh)	21 min 15 s
NOTE – Times are approximate	

5.1.3.5 Normal Outputs

Table 14: Idle command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.3.6 Error Outputs

Table 15: Idle command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

5.1.3.7 Prerequisites

DRDY set to one

5.1.3.8 Description

The IDLE command allows the host to place the device in the idle mode and also set the Standby timer.

5.1.4 Idle Immediate

5.1.4.1 Command Code

E1h

5.1.4.2 Feature Set

Power Management Feature Set.

5.1.4.3 Protocol

Non-Data

5.1.4.4 Inputs

Table 16: Idle immediate command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Command	E1h							

Device register-

DEV shall specify the selected device.

5.1.4.5 Normal Outputs

Table 17: Idle immediate command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.4.6 Prerequisites

DRDY set to one

5.1.4.7 Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the idle mode.

5.1.5 **SMART** (Under Developing)

Individual SMART commands are identified by the value placed in the Feature register.

Table 18: SMART Feature register values

Value	Command
D0h	SMATR Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

5.1.5.1 SMART Read Data

5.1.5.1.1 Command Code

B0h with a Feature register value of D0h

5.1.5.1.2 Feature Set

Smart Feature Set

- Operation when the SMART feature set is implemented.

5.1.5.1.3 Protocol

PIO data-in

5.1.5.1.4 Inputs

Table 19: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.1.5.1.5 Normal Outputs

Table 20: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.1.6 Prerequisites

DRDY set to one. SMART enabled.

5.1.5.1.7 Description

This command returns the Device SMART data structure to the host.

Table 21: ID of SMART data structure

ID(Hex)	Description
E9	ECC Fail Record
EA	Average Erase Count, Max Erase Count
EB	Good Block Count, System Block Count

ID: E9h

Table 22: Smart command for ECC fail record information

Byte	Function	Description
0	ECC fail number	When failure bit is bigger than "ECC Fail number", this block will be marked as Bad Block.
1	Row address 3	Flash Block Address
2	Row address 2	Flash Block Address
3	Row address 1	Flash Block Address
4	Channel number of last ECC fail	NA
5	Bank number of last ECC fail	NA
6	Reserved	NA
7	Reserved	NA

ID: EAh

Table 23: Smart command for average/max erase count information

Byte	Function	Description
0	Average Erase Count (High Byte)	Average erase count of all blocks.
1	Average Erase Count	
2	Average Erase Count (Low Byte)	
3	Max Erase Count (High Byte)	Indicate a block which's erase count is the largest.
4	Max Erase Count	
5	Max Erase Count (Low Byte)	
6	Reserved	NA
7	Reserved	NA

- When the Maximum erase count is 255 bigger than average erase count, the wear-leveling will be executed.

ID: EBh

Table 24: Smart command for good/system block count information

Byte	Function	Description
0	Good Block Count (High Byte)	Total used blocks of SSD
1	Good Block Count	
2	Good Block Count (Low Byte)	
3	System(Free) Block Count (High Byte)	Free block of SSD. Free block has to be bigger than 20. When the free block count is less than 20, the SSD will be locked.
4	System(Free) Block Count (Low Byte)	
5	Reserved	NA
6	Reserved	NA
7	Reserved	NA

5.1.5.2 SMART ENABLE OPERATIONS(Under Developing)

5.1.5.2.1 Command Code

B0h with a Feature register value of D8h

5.1.5.2.2 Feature Set

Smart Feature Set

5.1.5.2.3 Protocol

Non-data

5.1.5.2.4 Inputs

Table 25: SMART Enable command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.1.5.2.5 Normal Outputs

Table 26: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.2.6 Prerequisites

DRDY set to one.

5.1.5.2.7 Description

This command enables access to all SMART capabilities within device.

5.1.5.3 SMART DISABLE OPERATIONS

5.1.5.3.1 Command Code

B0h with a Feature register value of D9h

5.1.5.3.2 Feature Set

Smart Feature Set

5.1.5.3.3 Protocol

Non-data

5.1.5.3.4 Inputs

Table 27: SMART DISABLE Command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

5.1.5.3.5 Normal Outputs

Table 28: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

5.1.5.3.6 Prerequisites

DRDY set to one. SMART enabled.

5.1.5.3.7 Description

This command disables all SMART capabilities within device.

5.1.3 Read Multiple

5.1.3.1 Command Code

C4h

5.1.3.2 Protocol

PIO data-in

5.1.3.3 Inputs

Table 29: Read multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.3.4 Normal Output

Table 30: Read multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.3.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 31: Read multiple command for error output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.3.6 Prerequisites

DRDY set to one.

5.1.3.7 Description

This command reads the number of sectors specified in the sector Count register.

The number of sectors per block is defined by the content of word 59 in the IDENTIFY **DEVICE** response.

5.1.4 Read Sector(s)

5.1.4.1 Command Code

20h

5.1.4.2 Protocol

PIO data-in

5.1.4.3 Inputs

Table 32: Read sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	20h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.4.4 Normal Output

Table 33: Read sector command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.4.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 34: Read sector command for error outputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.4.6 Prerequisites

DRDY set to one.

5.1.4.7 Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. This transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High, and Device registers. The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition. The device shall interrupt for each DRQ block transferred.

5.1.5 Read Verify Sector

5.1.5.1 Command Code

40h

5.1.5.2 Protocol

Non-data

5.1.5.3 Inputs

Table 35: Read verify sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	40h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.5.4 Normal Output

Table 36: Read verify sector command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.5.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Table 37: Read verify sector command for normal output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.5.6 Prerequisites

DRDY set to one.

5.1.5.7 Description

This command is identical to the READ SECTOR(s) command, except that the device shall have read the data from the SSD, the DRQ bit is never set to one, and no data is transferred to the host.

5.1.6 Read DMA

5.1.6.1 Command Code

C8h

5.1.6.2 Protocol

DMA

5.1.6.3 Inputs

Table 38: Read DMA command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

5.1.6.4 Normal Output

5.1.6.5

Table 39: Read DMA command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.6.6 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 40: Read DMA command for error output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.6.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

5.1.6.8 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

5.1.7 Set Feature

TBD

5.1.8 Set Multiple Mode

5.1.8.1 Command Code

C6h

5.1.8.2 Protocol

Non-data

5.1.8.3 Inputs

If the content of the Sector Count Register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value in bits (7:0) in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1.

Table 41: Set multiple mode command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector per block							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	C6h							

5.1.8.4 Normal Output

Table 42: Set multiple mode command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.8.5 Error Outputs

Table 43: Set multiple mode command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	obs	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.8.6 Prerequisites

DRDY set to one.

5.1.8.7 Description

This command establishes the block count for READ MULTIPLE, READ MULTI EXT, WRITE MULTIPLE.

SSD can only support 1 sector per block.

5.1.9 Set Sleep Mode

5.1.9.1 Command Code

E6h

5.1.9.2 Protocol

Non-data

5.1.9.3 Inputs

Table 44: Set sleep mode for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E6h							

Device register–

DEV shall specify the selected device.

5.1.9.4 Normal Output

Table 45: Set sleep mode for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.9.5 Error Outputs

Table 46: Set sleep mode for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.9.6 Prerequisites

DRDY set to one.

5.1.9.7 Description

This command is the only way to cause the device to enter Sleep mode.

5.1.10 Flush Cache

5.1.10.1 Command Code

E7h

5.1.10.2 Protocol

Non-data

5.1.10.3 Inputs

Table 47: Flush cache command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

DEV shall specify the selected device.

5.1.10.4 Normal Output

Table 48: Flush cache command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.10.5 Error Outputs

Table 49: Flush cache command for error output information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.10.6 Prerequisites

DRDY set to one.

5.1.10.7 Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

5.1.11 Standby

5.1.11.1 Command Code

E2h

5.1.11.2 Protocol

Non-data

5.1.11.3 Inputs

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer.

Table 50: Standby command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Time period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E2h							

Device register–

DEV shall specify the selected device.

5.1.11.4 Normal Output

Table 51: Standby command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.11.5 Error Outputs

Table 52: Standby command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.11.6 Prerequisites

DRDY set to one.

5.1.11.7 Description

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then Standby timer shall be enabled. The value in the Sector Count register shall be used determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.

5.1.12 Standby Immediate

5.1.12.1 Command Code

E0h

5.1.12.2 Protocol

Non-data

5.1.12.3 Inputs

Table 53: Standby immediate command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							

LBA Low	Na				
LBA Mid	Na				
LBA High	Na				
Device	obs	Na	obs	DEV	Na
Command	E0h				

Device register–

DEV shall specify the selected device.

5.1.12.4 Normal Output

Table 54: Standby immediate command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.12.5 Error Outputs

Table 55: Standby immediate command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.12.6 Prerequisites

DRDY set to one.

5.1.12.7 Description

This command causes the device to immediately enter the Standby mode.

5.1.13 Write Multiple

5.1.13.1 Command Code

C5h

5.1.13.2 Protocol

PIO data-out

5.1.13.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 56: Write multiple command for inputs information

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.1.13.4 Normal Output

Table 57: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.13.5 Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 58: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible

address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.13.6 Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

5.1.13.7 Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
N = Remainder (sector count / block count).

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.
The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

5.1.14 Write Sector

5.1.14.1 Command Code

30h

5.1.14.2 Protocol

PIO data-out

5.1.14.3 Inputs

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 59: Write sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	30h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

5.1.14.4 Normal Output

Table 60: Write sector command for inputs information

Register	7	6	5	4	3	2	1	0
Error	**Na**							
Sector Count	**Na**							
LBA Low	**Na**							
LBA Mid	**Na**							

LBA High	**Na**							
Device	**obs**	**Na**	**obs**	**DEV**	**Na**	**Na**	**Na**	**Na**
Status	**BSY**	**DRDY**	**DF**	**Na**	**DRQ**	**Na**	**Na**	**ERR**

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.14.5 Error Outputs

An unrecoverable error encountered during the execution if this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 61: Write sector command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.14.6 Prerequisites

DRDY set to one.

5.1.14.7 Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The device shall interrupt for each DRQ block transferred.

5.1.15 Write DMA

5.1.15.1 Command Code

CAh

5.1.15.2 Protocol

DMA

5.1.15.3 Inputs

The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 62: Write DMA command for input information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	CAh							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits (3:0) starting LBA bits (27:24**)**

Normal Output

Table 63: Write DMA command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

5.1.15.4 Error Outputs

Table 64: Write DMA command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

IDNF shall be set to one if a user-accessible address could not be found. INDF shall be set to one if an address outside of the range of user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.15.5 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

5.1.15.6 Description

The Write DMA command allows the host to write data using the DMA data transfer protocol.

5.1.16 Execute Device Diagnostic

5.1.16.1 Command Code

90h

5.1.16.2 Feature Set

General feature set

5.1.16.3 Protocol

Device diagnostic

5.1.16.4 Inputs

Only the command code (90h). All other registers shall be ignored.

Table 65: Execute device diagnostic command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	90h							

Device –

DEV shall be ignored.

Normal Outputs

The diagnostic code written into the Error register is an 8-bit code.

Table 66: Execute device diagnostic command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Diagnostic Code							
Sector Count	Signature							
LBA Low	Signature							
LBA Mid	Signature							
LBA High	Signature							
Device	Signature							
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

Diagnostic Code

Sector Count, LBA Low, LBA Mid, LBA High, Device registers

Device signature

Device register

DEV shall be cleared to zero.

Status register

TBD

Table 67: Execute device diagnostic command for status register information

Code	Description
01h	Device passed
Others	Device failed

5.1.16.5 Error Outputs

Table 9 shows the error information that is returned as a diagnostic code in the Error register.

5.1.16.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

5.1.16.7 Description

This command shall cause the devices to perform the internal diagnostic tests.

5.1.17 **Security Set Password** (Under Developing)

5.1.17.1 Command Code

F1h

5.1.17.2 Feature Set

Security Mode feature set

5.1.17.3 Protocol

PIO data-out

5.1.17.4 Inputs

Table 68: Security set password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device –

DEV shall specify the selected device.

Normal Outputs

Table 69: Security set password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.1.17.5 Error Outputs

Table 70: Security set password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.17.6 Prerequisites

DRDY set to one.

5.1.17.7 Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this information. The data transferred controls the function of this command. Table 11 defines the interaction of the identifier and security level bits.

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Table 71: Security set password command's data content

Word	Content
0	Control Word Bit 0 Identifier 0=set User password 1=set Master password Bits (7:1) Reserved Bit(8) Security level 0=High 1=Maximum Bits(15:9) Reserved
1-16	Password(32 bytes)
17	Master Password Revision Code()
18-255	Reserved

Table 72: Security Set password command's identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall than be unlocked by either the User password it the previously set Master password.

User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

5.1.18 Security Unlock(Under Developing)

5.1.18.1 Command Code

F2h

5.1.18.2 Feature Set

Security Mode feature set

5.1.18.3 Protocol

PIO data-out

5.1.18.4 Inputs

Table 73: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F2h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 74: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.1.18.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 75: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.18.6 Prerequisites

DRDY set to one.

5.1.18.7 Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

5.1.19 Security Erase Prepare(Under Developing)

5.1.19.1 Command Code

F3h

5.1.19.2 Feature Set

Security Mode feature set

5.1.19.3 Protocol

Non-data

5.1.19.4 Inputs

Table 76: Security erase prepare command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F3h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 77: Security erase prepare command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

5.1.19.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 78: Security erase prepare command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.19.6 Prerequisites

DRDY set to one.

5.1.19.7 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

5.1.20 Security Erase Unit(Under Developing)

5.1.20.1 Command Code

F4h

5.1.20.2 Feature Set

Security Mode feature set

5.1.20.3 Protocol

PIO data-out.

5.1.20.4 Inputs

Table 79: Security erase unit command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 80: Security erase unit command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.1.20.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 81: Security erase unit command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.20.6 Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

5.1.20.7 Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is set.

Table 82: Security erase unit password information

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit 1 Erase mode 0=Normal Erase 1=Enhanced Erase Bit(15:2) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

5.1.21 Security Freeze Lock

5.1.21.1 Command Code

F5h

5.1.21.2 Feature Set

Security Mode feature set

5.1.21.3 Protocol

Non-data.

5.1.21.4 Inputs

Table 83: Security freeze lock for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 84: Security freeze lock for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							

LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.1.21.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 85: Security freeze lock for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.21.6 Prerequisites

DRDY set to one.

5.1.21.7 Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECUIRTY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

5.1.22 Security Disable Password(Under Developing)

5.1.22.1 Command Code

F6h

5.1.22.2 Feature Set

Security Mode feature set

5.1.22.2.1 Protocol

PIO data-out.

5.1.22.3 Inputs

Table 86: Security disable password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 87: Security disable password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

5.1.22.4 Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

Table 88: Security disable password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

5.1.22.5 Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

5.1.22.6 Description

The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. Table 13 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated

when a User password if set.

Table 89: Security disable password command content

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit(15:1) Reserved
1-16	Password (32 Bytes)
17-255	Reserved