InnoDisk SATA Slim J80 Datasheet

Rev. 1.0

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REVISION HISTORY

Revision	Description	Date
Preliminary	First released	Apr. 2010
Rev. 1.0	Model Name Changed to SATA Slim J80	Jul. 2010

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1. Product Introduction

1.1. Overview

InnoDisk SATA Slim J80 is designed to comply with JEDEC SFF-8156 standard form factor, which is extremely suitable for portable / hand-held devices or thin clients. Moreover, its standard 7+15 pin SATA interface could support most of the platform with standard SATA port. InnoDisk SATA Slim J80 operates under SATA II (3.0Gb/s) protocol with good performance, the sustain read/write can reach up to 90/60MB per second (max).

InnoDisk SATA Slim J80 is also suitable in industrial field. It effectively reduces the booting time of operation system and the power consumption is less than hard disk drive (HDD). InnoDisk SATA Slim J80 complies with ATA protocol, no additional drivers are required, and the SATA Slim can be configured as a boot device or data storage device.

1.2. Product Picture

Figure 1: InnoDisk SATA Slim J80 picture

1.3. Product Features

- Interface: Serial ATA II (3.0Gbps)
- Capacity: 2GB~16GB
- Data transfer rate:
- Read- 90 MB/sec. (max.), Write- 60MB/sec. (max.)
- Access time: 0.3ms
- Error Correction Function
- Built-in ECC corrects up to 8-bit per 512-Byte

- Dimension: 54.0 x 39.0 x 4.0mm

2. Specifications

2.1. Environmental Specifications

2.1.1. Temperature Range

- Operating Temperature Range
  - Standard Grade: 0°C to +70°C
- Storage Temperature Range
  - Standard / Industrial Grade: -55°C to +95°C

2.1.2. Humidity

Relative Humidity: 10-95%, non-condensing

2.1.3. Shock and Vibration

Table 1: Shock/Vibration Testing for InnoDisk SATA Slim J80

Reliability	Test Conditions
Vibration	7 to 2000 Hz, 20G, 3 axes
Mechanical Shock	Duration: 10ms, 50G, 3 axes

2.2. System Reliability

2.2.1. ECC Technology

High reliability based on the internal error correct code (ECC) function. Built-in ECC corrects up to 8-bit per 512-Byte.

2.2.2. Mean Time between Failures (MTBF)

Table 2 summarizes the MTBF prediction results for various InnoDisk SATA Slim J80 configurations. The analysis is performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 2: InnoDisk SATA Slim J80 MTBF

Product	Condition	MTBF (Hours)
InnoDisk SATA Slim J80	Telcordia SR-332 GB, 25°C	> 3,000,000

2.2.3. Transfer Mode

InnoDisk SATA Slim J80 supports the following transfer mode:

- PIO Mode: 0~4
- Multiword DMA: 0~2
- Ultra DMA: 0~6

2.3. Power Requirement

2.3.1. DC Input Voltage

5V (±5%) single power supply operation

2.3.2. Power Consumption

Table 3: InnoDisk SATA Slim J80 power consumption (max.)

Parameter	mA
Sustained Read	250
Sustained Write	300
IDLE	150

2.4. Certificate

2.4.1. CE and FCC Compatibility

InnoDisk SATA Slim J80 conforms to CE and FCC requirements.

2.4.2. RoHS Compliance

InnoDisk SATA Slim J80 is fully compliant with RoHS directive.

3. Theory of operation

3.1. Overview

Figure 2 shows the operation of InnoDisk SATA Slim J80 from the system level, including the major hardware blocks. As the diagram shown, SATA II controller communicates with SATA II host interface directly. Also SATA II controller supports one flash IC.

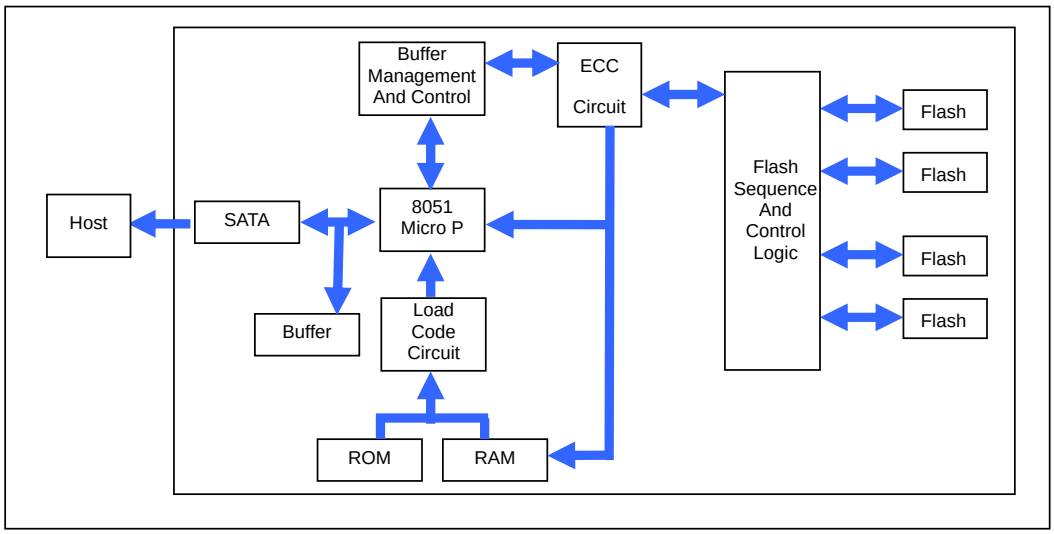

Figure 2: InnoDisk SATA Slim J80 Block Diagram

3.2. SATA II Controller

The SATA II controller is 3.0Gbps, and supports hot-plug. This SATA II controller support four flash IC and communicates with host interface, this SATA II controller can support the flash ICs for 4kbyte per page.

3.3. Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 8 bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

3.4. Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

InnoDisk SATA Slim J80 uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page and block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

3.5. Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SATA Slim is shipped, or may develop during the life time of the SSD. The Bad Blocks will not exceed more than 6.7% of the total device volume. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SATA Slim implement Bad Blocks management, Bad Block replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

4. Installation Requirements

4.1. SATA Slim Pin Directions

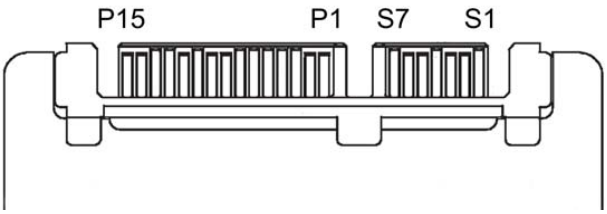

Figure 3: Signal Segment and Power Segment

4.2. Device driver

No additional device drivers are required. The InnoDisk SATA Slim J80 can be configured as a boot device.

5. Specifications

5.1. Pin Assignment

InnoDisk SATA Slim J80 is designed within SATA II Interface. Particularly, its built-in power pin enables the device more compactable. Table 4 demonstrates InnoDisk SATA Slim J80 pin assignments.

Table 4: InnoDisk SATA Slim J80 Pin Assignment

Name	Type	Description
S1	GND	NA
S2	A+	Differential Signal Pair A
S3	A-	
S4	GND	NA
S5	B-	Differential Signal Pair B
S6	B+	
S7	GND	NA
Key and Spacing separate signal and power segments		
P1	V33	3.3V Power
P2	V33	3.3V Power
P3	V33	3.3V Power, Pre-charge
P4	GND	NA
P5	GND	NA
P6	GND	NA
P7	V5	5V Power, Pre-Charge
P8	V5	5V Power
P9	V5	5V Power
P10	GND	NA
P11	DAS/DSS	Device Activity Signal / Disable Staggered Spinup
P12	GND	NA
P13	V12	12V Power, Pre-charge
P14	V12	12V Power
P15	V12	12V Power

5.2. Mechanical Dimensions

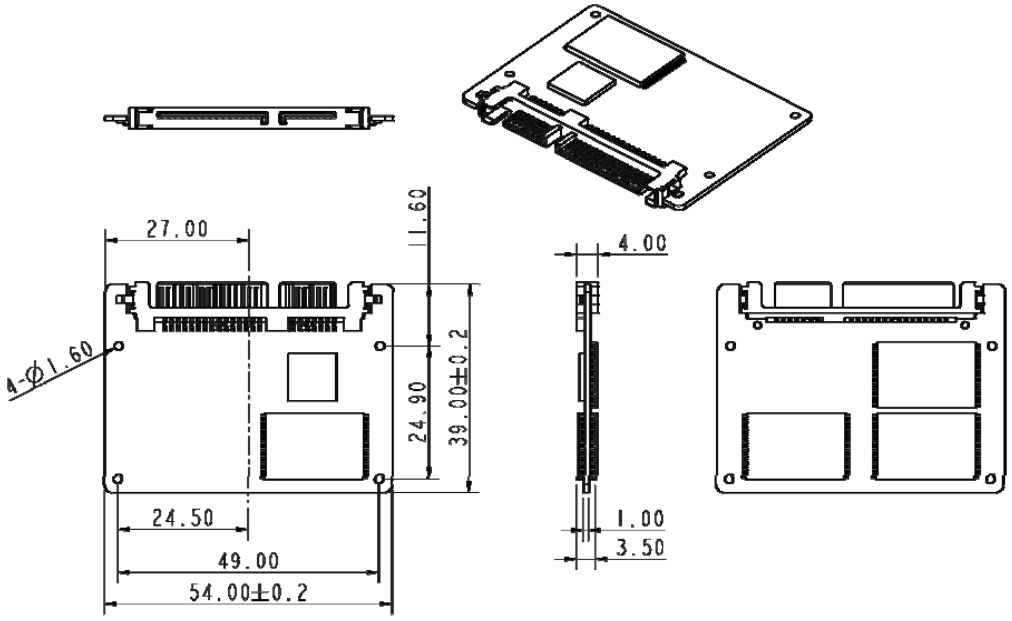

Figure 4: InnoDisk SATA Slim J80 mechanical dimensions

5.3. Performance

A. Burst Speed Rate: 300MB/sec.

B. Data Transfer Rate

- Sustained Read: 90MB/sec (max.)
- Sustained Write: 60MB/sec (max.)

5.4. Seek Time

InnoDisk SATA Slim J80 is not a magnetic rotating design. There is no seek or rotational latency required.

5.5. NAND Flash Memory

InnoDisk SATA Slim J80 uses Single Level Cell (SLC) NAND and, which are non-volatility, high reliability and high speed memory storage.

6. Supported ATA Commands

InnoDisk SATA Slim J80 supports the commands listed in Table 5.

Table 5: ATA Commands

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
SMART	B0h	X	X	O	O	X	O
READ MULTIPLE	C4h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
READ DMA	C8h or C9h	O	O	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
SEEK	7xh	X	X	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X

SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
READ BUFFER	E4h	X	X	X	X	O	X
WRITE BUFFER	E8h	X	X	X	X	O	X

6.1. Check Power Mode- E5h

Table 6: Check power mode command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E5h							

Device register

DEV shall specify the selected device.

6.2. IDENTIFY DEVICE- ECh

Table 7: Identify device command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	Obs	DEV	Na	Na	Na	Na
Command	ECh							

Device register

DEV shall specify the selected device.

Outputs

Normal outputs

Table 8: Identify device command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion.

DRDY shall be set to one.

DF (Device Fault) shall be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one.

Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device. When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and asserts INTRQ if nIEN is cleared to zero. The host may then transfer the data by reading the Data register. Table 8 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a 16-bit value. A word that is defined as a 16-bit value places the most significant bit of the value on signal line DD15 and the least significant bit on signal line DD0. Some parameters are defined as 32-bit values (e.g. words (61:60)). Such fields are transfer using two successive word transfers. The device will first transfer the least significant bits, bits (15:0) of the value, on signal lines DD(15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits(31:16) of the value, shall be transferred on DD(15:0) respectively.

Some parameters are defined as a string of ASCII characters.

Table 9: Identify device command parameters

Word	Description	Value
0	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved	0040h
1	Obsolete	XXXXh
2	Specific configuration	C837h
3	Obsolete	0010h
4-5	Retired	0000h
6	Obsolete	003Fh
7-8	Reserved for assignment by the CompactFlash™ Association	0000h
9	Retired	0000h
10-19	Serial number (20 ASCII characters)	20 ASCII characters
20-21	Retired	0000h
22	Obsolete	0000h
23-26	Firmware revision (8 ASCII characters)	8 ASCII characters
27-46	Model number (40 ASCII characters)	40 ASCII characters
47	15-8 80h 7-0 00h = Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	8001h
48	Reserved	0000h
49	Capabilities 15-1 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command.	2F00h

	11	1 = IORDY supported 0 = IORDY may be supported	
	10	1 = IORDY may be disabled	
	9	1 = LBA supported	
	8	1 = DMA supported.	
	7-0	Retired	
50	Capabilities 15 14: 13-2 1 0	Shell be cleared to zero Shall be set to one Reserved Obsolete Shall be set to one to indicate a device specific Standby timer value minimum.	4000h
51-52	Obsolete		0000h
53	15-3 2 1 0	Reserved 1 = the fields reported in word 88 are valid Reserved 0 = the fields reported in word 88 are not valid 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid Obsolete	0007h
54	Number of current logical cylinders		XXXXh
55	Number of current logical heads		XXXXh
56	Number of current logical sectors per logical track		XXXXh
57-58	Current capacity in sectors		XXXXh
59	15-9 8 7-0	Reserved 1 = Multiple sector setting is valid xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	0101h
60-61	Total number of user addressable sectors		XXXXXXXXh
62	Obsolete		0000h
63	15-11 10 9 8	Reserved 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 1 = Multiword DMA mode 0 is selected	XX07h

		0 = Multiword DMA mode 0 is not selected	
	7-3	Reserved	
	2	1 = Multiword DMA mode 2 and below are supported	
	1	1 = Multiword DMA mode 1 and below are supported	
	0	1 = Multiword DMA mode 0 is supported	
64	15-8	Reserved	0003h
	7-0	PIO modes supported	
65	Minimum Multiword DMA transfer cycle time per word		0078h
	15-0	Cycle time in nanoseconds	
66	Manufacturer's recommended Multiword DMA transfer cycle time		0078h
	15-0	Cycle time in nanoseconds	
67	Minimum PIO transfer cycle time without flow control		0078h
	15-0	Cycle time in nanoseconds	
68	Minimum PIO transfer cycle time with IORDY flow control		0078h
	15-0	Cycle time in nanoseconds	
69-70	Reserved (for future command overlap and queuing)		0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.		0000h
75	Queue depth		0000h
	15-5	Reserved	
	4-0	Maximum queue depth - 1	
76-79	Reserved for Serial ATA		0006h
80	Major version number 0000h or FFFFh = device does not report version		00F0h
	15	Reserved	
	14	Reserved for ATA/ATAPI-14	
	13	Reserved for ATA/ATAPI-13	
	12	Reserved for ATA/ATAPI-12	
	11	Reserved for ATA/ATAPI-11	
	10	Reserved for ATA/ATAPI-10	
	9	Reserved for ATA/ATAPI-9	
	8	Reserved for ATA/ATAPI-8	
	7	1 = supports ATA/ATAPI-7	
	6	1 = supports ATA/ATAPI-6	
	5	1 = supports ATA/ATAPI-5	
	4	1 = supports ATA/ATAPI-4	
	3	Obsolete	
	2	Obsolete	

	1	Obsolete	
	0	Reserved	
81	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = See 6.17.41		0000h
82	Command set supported.		304Bh
	15	Obsolete	
	14	1 = NOP command supported	
	13	1 = READ BUFFER command supported	
	12	1 = WRITE BUFFER command supported	
	11	Obsolete	
	10	1 = Host Protected Area feature set supported	
	9	1 = DEVICE RESET command supported	
	8	1 = SERVICE interrupt supported	
	7	1 = release interrupt supported	
	6	1 = look-ahead supported	
	5	1 = write cache supported	
	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	
	3	1 = mandatory Power Management feature set supported	
	2	1 = Removable Media feature set supported	
	1	1 = Security Mode feature set supported	
	0	1 = SMART feature set supported	
83	Command sets supported.		5000h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = mandatory FLUSH CACHE command supported	
	11	1 = Device Configuration Overlay feature set supported	
	10	1 = 48-bit Address feature set supported	
	9	1 = Automatic Acoustic Management feature set supported	
	8	1 = SET MAX security extension supported	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spinup after power-up	
	5	1 = Power-Up In Standby feature set supported	
	4	1 = Removable Media Status Notification feature set supported	

	3	1 = Advanced Power Management feature set supported	
	2	1 = CFA feature set supported	
	1	1 = READ/WRITE DMA QUEUED supported	
	0	1 = DOWNLOAD MICROCODE command supported	
84	Command set/feature supported extension		4000h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report	
	11	Reserved for technical report	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64-bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Streaming feature set supported	
	3	1 = Media Card Pass Through Command feature set supported	
	2	1 = Media serial number supported	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
85	Command and feature sets supported or enabled		
	15	Obsolete	0
	14	1 = NOP command enabled	0
	13	1 = READ BUFFER command enabled	1
	12	1 = WRITE BUFFER command enabled	1
	11	Obsolete	0
	10	1 = Host Protected Area feature set enabled	0
	9	1 = DEVICE RESET command enabled	0
	8	1 = SERVICE interrupt enabled	0
	7	1 = release interrupt enabled	0
	6	1 = look-ahead enabled	X
	5	1 = Write Cache enabled	X

	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	0
	3	1 = Power Management feature set enabled	1
	2	1 = Removable Media feature set enabled	0
	1	1 = Security Mode feature set enabled	X
	0	1 = SMART feature set enabled	X
86	Command set/feature enabled		1000h
	15-14	0 = Reserved	
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = FLUSH CACHE command supported	
	11	1 = Device Configuration Overlay supported	
	10	1 = 48-bit Address features set supported	
	9	1 = Automatic Acoustic Management feature set enabled	
	8	1 = SET MAX security extension enabled by SET MAX SET PASSWORD	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spin-up after power-up	
	5	1 = Power-Up In Standby feature set enabled	
	4	1 = Removable Media Status Notification feature set enabled	
	3	1 = Advanced Power Management feature set enabled	
	2	1 = CFA feature set enabled	
	1	1 = READ/WRITE DMA QUEUED command supported	
	0	1 = DOWNLOAD MICROCODE command supported	
87	Command and feature sets supported or enabled		4000h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report-	
	11	Reserved for technical report-	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64 bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT	

		commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Valid CONFIGURE STREAM command has been executed	
	3	1 = Media Card Pass Through Command feature set enabled	
	2	1 = Media serial number is valid	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
88	15	Reserved	XX7Fh
	14	1 = Ultra DMA mode 6 is selected	
		0 = Ultra DMA mode 6 is not selected	
	13	1 = Ultra DMA mode 5 is selected	
		0 = Ultra DMA mode 5 is not selected	
	12	1 = Ultra DMA mode 4 is selected	
		0 = Ultra DMA mode 4 is not selected	
	11	1 = Ultra DMA mode 3 is selected	
		0 = Ultra DMA mode 3 is not selected	
	10	1 = Ultra DMA mode 2 is selected	
		0 = Ultra DMA mode 2 is not selected	
	9	1 = Ultra DMA mode 1 is selected	
		0 = Ultra DMA mode 1 is not selected	
	8	1 = Ultra DMA mode 0 is selected	
		0 = Ultra DMA mode 0 is not selected	
	7	Reserved	
	6	1 = Ultra DMA mode 6 and below are supported	
	5	1 = Ultra DMA mode 5 and below are supported	
	4	1 = Ultra DMA mode 4 and below are supported	
	3	1 = Ultra DMA mode 3 and below are supported	
	2	1 = Ultra DMA mode 2 and below are supported	
	1	1 = Ultra DMA mode 1 and below are supported	
	0	1 = Ultra DMA mode 0 is supported	
89	Time required for security erase unit completion		0001h
90	Time required for Enhanced security erase completion		0001h
91	Current advanced power management value		0000h
92	Master Password Revision Code		FFFEh
93	Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset.		XXXXh
	15	Shall be cleared to zero.	

	14	Shall be set to one.	
	13	1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL	
	12-8	Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows: 12 Reserved. 11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-. 10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 8 Shall be set to one.	
	7-0	Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows: 7 Reserved. 6 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected. 5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-. 4 0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-. 3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics. 2-1 These bits indicate how Device 0 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 0 Shall be set to one.	
94	15-8 7-0	Vendor's recommended acoustic management value. Current automatic acoustic management value.	0000h
95	Stream Minimum Request Size		0000h
96	Streaming Transfer Time - DMA		0000h
97	Streaming Access Latency - DMA and PIO		0000h

98-99	Streaming Performance Granularity		0000h
100-103	Maximum user LBA for 48-bit Address feature set.		0000h
104	Streaming Transfer Time - PIO		0000h
105	Reserved		0000h
106	Physical sector size / Logical Sector Size		4000h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = Device has multiple logical sectors per physical sector.	
	12	1= Device Logical Sector Longer than 256 Words	
	11-4	Reserved	
	3-0	2^X logical sectors per physical sector	
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds		0000h
108	15-12	NAA (3:0)	0000h
	11-0	IEEE OUI (23:12)	
109	15-4	IEEE OUI (11:0)	0000h
	3-0	Unique ID (35:32)	
110	15-0	Unique ID (31:16)	0000h
111	15-0	Unique ID (15:0)	0000h
112-115	Reserved for world wide name extension to 128 bits		0000h
116	Reserved for technical report-		0000h
117-118	Words per Logical Sector		0000h
119-120	Reserved		4000h
121-126	Reserved		0000h
127	Removable Media Status Notification feature set support		0000h
	15-2	Reserved	
	1-0	00 = Removable Media Status Notification feature set not supported	
		01 = Removable Media Status Notification feature supported	
		10 = Reserved	
		11 = Reserved	

128	Security Status		
	15-9	Reserved	0
	8	Security level 0 = high, 1 = Maximum	X
	7-6	Reserved	0
	5	1= Enhanced security erase supported	1
	4	1= Security count expired	X
	3	1 = Security frozen	X
	2	1 = Security locked	X
	1	1 = Security enabled	X
	0	1 = Security supported	1
129-159	Vendor specific		3D3Dh
160	CFA power mode 1		
	15	Word 160 supported	
	14	Reserved	
	13	CFA power mode 1 is required for one or more commands implemented by the device	0000h
	12	CFA power mode 1 disabled	
	11-0	Maximum current in ma	
161-175	Reserved for assignment by the CompactFlash™ Association		0000h
176-205	Current media serial number		0000h
206-254	Reserved		0000h
255	Integrity word		
	15-8	Checksum	XXXXh
	7-0	Signature	

6.3. IDLE- E3h

Table 10: Idle command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Timer period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	Obs	DEV	Na	Na	Na	Na
Command	E3h							

Device register-

DEV shall specify the selected device.

Table 11: Idle command sector count register contents information

Sector Count register contents	Corresponding timeout period
0 (00h)	Timeout disabled
1-240 (01h-F0h)	(value*5)s
241-251 (F1h-FBh)	((Value-240)*30)min
252 (FCh)	21min
253 (FDh)	Period between 8 and 12 hrs
254 (FEh)	Reserved
255 (FFh)	21 min 15 s
NOTE – Times are approximate	

Normal Outputs

Table 12: Idle command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Error Outputs

Table 13: Idle command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							

LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Prerequisites

DRDY set to one

Description

The IDLE command allows the host to place the device in the idle mode and also set the Standby timer.

6.4. Idle Immediate- E1h

Table 14: Idle immediate command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Command	E1h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 15: Idle immediate command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one

Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the idle mode.

6.5. SMART-B0h

Individual SMART commands are identified by the value placed in the Feature register.

Table 16: SMART Feature register values

Value	Command
D0h	SMATR Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

6.5.1. SMART Read Data- D0h

Table 17: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 18: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one. SMART enabled.

Description

This command returns the Device SMART data structure to the host.

Table 19: ID of SMART data structure

ID(Hex)	Description
E9	ECC Fail Record
EA	Average Erase Count, Max Erase Count
EB	Good Block Count, System Block Count

ID: E9h

Table 20: Smart command for ECC fail record information

Byte	Function	Description
0	ECC fail number	When failure bit is bigger than “ECC Fail number”, this block will be marked as Bad Block.
1	Row address 3	Flash Block Address
2	Row address 2	Flash Block Address
3	Row address 1	Flash Block Address
4	Channel number of last ECC fail	NA
5	Bank number of last ECC fail	NA
6	Reserved	NA
7	Reserved	NA

ID: EAh

Table 21: Smart command for average/max erase count information

Byte	Function	Description
0	Average Erase Count (High Byte)	Average erase count of all blocks.
1	Average Erase Count	
2	Average Erase Count (Low Byte)	
3	Max Erase Count (High Byte)	Indicate a block which's erase count is the largest.
4	Max Erase Count	
5	Max Erase Count (Low Byte)	
6	Reserved	NA
7	Reserved	NA

ID: EBh

Table 22: Smart command for good/system block count information

Byte	Function	Description
0	Good Block Count (High Byte)	Total used blocks of SSD
1	Good Block Count	
2	Good Block Count (Low Byte)	
3	System(Free) Block Count (High Byte)	Free block of SSD. Free block has to be bigger than 20. When the free block count is less than 20, the SSD will be locked.
4	System(Free) Block Count (Low Byte)	
5	Reserved	NA
6	Reserved	NA
7	Reserved	NA

6.5.2. SMART ENABLE OPERATIONS

Table 23: SMART Enable command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 24: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one.

Description

This command enables access to all SMART capabilities within device.

6.5.3. SMART DISABLE OPERATIONS

Table 25: SMART DISABLE Command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

Normal Outputs

Table 26: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

Prerequisites

DRDY set to one. SMART enabled.

Description

This command disables all SMART capabilities within device.

6.6. Read Multiple- C4h

Table 27: Read multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

Normal Output

Table 28: Read multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 29: Read multiple command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							

LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command reads the number of sectors specified in the sector count register. The number of sectors per block is defined by the content of word 59 in the IDENTIFY DEVICE response.

6.7. Read Sector(s)- 20h

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

Normal Output

Table 30: Read sector command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 31: Read sector command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address is requested could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. This transfer shall begin at the sector specified in the LBA Low, LBA Mid, LBA High, and Device registers. The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition. The device shall interrupt for each DRQ block transferred.

6.8. Read Verify Sector- 40h

Table 32: Read verify sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	40h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

Normal Output

Table 33: Read verify sector command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Table 34: Read verify sector command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			

Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command is identical to the READ SECTOR(s) command, except that the device shall have read the data from the SSD, the DRQ bit is never set to one, and no data is transferred to the host.

6.9. Read DMA- C8h

Table 35: Read DMA command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C4h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors are to be transferred.

LBA Low-

Starting LBA bits (7:0).

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

DEV shall specify the selected device.

Bit (3:0) starting LBA bits (27:24)

Normal Output

Table 36: Read DMA command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred us indeterminate.

Table 37: Read DMA command for error output information

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			

Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable.

IDNF shall be set to one if a user-accessible address could not be found.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

6.10. Set Multiple Mode- C6h

If the content of the Sector Count Register is not zero, then the Sector Count register contains the number of sectors per block for the device to be used on all following READ/WRITE MULTIPLE commands. The content of the Sector Count register shall be less than or equal to the value in bits (7:0) in word 47 in the IDENTIFY DEVICE information. The host should set the content of the Sector Count register to 1.

Table 38: Set multiple mode command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector per block							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	C6h							

Normal Output

Table 39: Set multiple mode command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 40: Set multiple mode command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	obs	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command establishes the block count for READ MULTIPLE, READ MULTI EXT, WRITE MULTIPLE.

SSD can only support 1 sector per block.

6.11. Set Sleep Mode- E6h

Table 41: Set sleep mode for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E6h							

Device register–

DEV shall specify the selected device.

Normal Output

Table 42: Set sleep mode for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 43: Set sleep mode for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command is the only way to cause the device to enter Sleep mode.

6.12. Flush Cache- E7h

Table 44: Flush cache command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E7h							

Device register–

DEV shall specify the selected device.

Normal Output

Table 45: Flush cache command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 46: Flush cache command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command is used by the host to request the device to flush the write cache. If there is data in write cache, that data shall be written to the SSD. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

6.13. Standby- E2h

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer.

Table 47: Standby command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Time period value							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E2h							

Device register–

DEV shall specify the selected device.

Normal Output

Table 48: Standby command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 49: Standby command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then Standby timer shall be enabled. The value in the Sector Count register shall be used determine the time programmed into the Standby timer. If the Sector Count register is zero then the Standby timer is disabled.

6.14. Standby Immediate- E0h

Table 50: Standby immediate command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							

Sector Count	Na				
LBA Low	Na				
LBA Mid	Na				
LBA High	Na				
Device	obs	Na	obs	DEV	Na
Command	E0h				

Device register–

DEV shall specify the selected device.

Normal Output

Table 51: Standby immediate command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 52: Standby immediate command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			

Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT may be set to one if the device is not able to complete the action requested by the command.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command causes the device to immediately enter the Standby mode.

6.15. Write Multiple- C5h

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 53: Write multiple command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	Na	obs	DEV	LBA(27:24)			
Command	C5h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

Normal Output

Table 54: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block register contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 55: Write multiple command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							

LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, include an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if an address outside of the range of user-accessible address is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device -

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. If bit 8 of IDENTIFY DEVICE word 59 is cleared to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

Description

This command writes the number of sectors specified in the Sector Count register.

The number of sectors per block is defined by the content of word 59 of the IDENTIFY DEVICE response.

When the WRITE MULTIPLE command is issued, the SECTOR Count register contains the number of sectors (not the number of blocks) requested. The device shall interrupt for each DRQ block transferred.

IF the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final,

partial block transfer. The partial block transfer is for n sectors, where: N = Remainder (sector count / block count).

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with command aborted.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The command ends with the sector in error, even if the error was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block that had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupt pending is set when the DRQ bit is set to one at the beginning of each block or partial block.

6.16. Write Sector- 30h

The LBA mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 56: Write sector command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	obs	LBA	obs	DEV	LBA(27:24)			
Command	30h							

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits(3:0) starting LBA bits (27:24)

Normal Output

Table 57: Write sector command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

An unrecoverable error encountered during the execution if this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminate.

Table 58: Write sector command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	WP	MC	IDNF	MCR	ABRT	NM	Na
Sector Count	Na							
LBA Low	LBA(7:0)							

LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

IDNF shall be set to one if a user-accessible address could not be found. IDNF shall be set to one if an address outside of the range of user-accessible addresses is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The device shall interrupt for each DRQ block transferred.

6.17. Write DMA- CAh

The LBA Mid, LBA High, Device, and LBA Low specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Table 59: Write DMA command for input information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Sector Count							
LBA Low	LBA(7:0)							

LBA Mid	LBA(15:8)				
LBA High	LBA(23:16)				
Device	obs	LBA	obs	DEV	LBA(27:24)
Command	CAh				

Sector Count-

Number of sectors to be transferred. A value of 00h specifies that 256 sectors shall be transferred.

LBA Low-

Starting LBA bits (7:0)

LBA Mid-

Starting LBA bits (15:8)

LBA High-

Starting LBA bits (23:16)

Device –

The LBA bit shall be set to one to specify the address is an LBA.

DEV shall specify the selected device.

Bits (3:0) starting LBA bits (27:24)

Normal Output

Table 60: Write DMA command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

Table 61: Write DMA command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	ICRC	WP	MC	IDNF	MCR	ABRT	NM	Obs
Sector Count	Na							
LBA Low	LBA(7:0)							
LBA Mid	LBA(15:8)							
LBA High	LBA(23:16)							
Device	Obs	Na	obs	DEV	LBA(27:24)			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

IDNF shall be set to one if a user-accessible address could not be found. INDF shall be set to one if an address outside of the range of user-accessible address is requested if command aborted is not returned.

ABRT shall be set to one if an error, including an ICRC error, has occurred during an Ultra DMA data transfer. ABRT shall be set to one if the device is not able to complete the action requested by the command. ABRT shall be set to one if an address outside of the range of user-accessible addresses is requested if IDNF is not set to one.

LBA Low, LBA Mid, and LBA High, Device

Shall be written with the address of first unrecoverable error.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

Description

The Write DMA command allows the host to write data using the DMA data transfer protocol.

6.18. Execute Device Diagnostic- 90h

Table 62: Execute device diagnostic command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	90h							

Device –

DEV shall be ignored.

Normal Outputs

The diagnostic code written into the Error register is an 8-bit code.

Table 63: Execute device diagnostic command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Diagnostic Code							
Sector Count	Signature							
LBA Low	Signature							
LBA Mid	Signature							
LBA High	Signature							
Device	Signature							
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

Diagnostic Code

Sector Count, LBA Low, LBA Mid, LBA High, Device registers

Device signature

Device register

DEV shall be cleared to zero.

Status register

TBD

Table 64: Execute device diagnostic command for status register information

Code	Description
01h	Device passed
Others	Device failed

Error Outputs

Table 9 shows the error information that is returned as a diagnostic code in the Error register.

Prerequisites

This command shall be accepted regardless of the state of DRDY.

Description

This command shall cause the devices to perform the internal diagnostic tests.

6.19. Security Set Password- 91h

Table 65: Security set password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device –

DEV shall specify the selected device.

Normal Outputs

Table 66: Security set password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

Error Outputs

Table 67: Security set password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this information. The data transferred controls the function of this command. Table 11 defines the interaction of the identifier and security level bits.

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Table 68: Security set password command's data content

Word	Content
0	Control Word Bit 0 Identifier 0=set User password

	1=set Master password Bits (7:1) Reserved Bit(8) Security level 0=High 1=Maximum Bits(15:9) Reserved
1-16	Password(32 bytes)
17	Master Password Revision Code()
18-255	Reserved

Table 69: Security Set password command's identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall than be unlocked by either the User password it the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

6.20. Security Unlock- F2h

Table 70: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	Na	Na
Command	F2h				

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 71: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

Error Outputs

The device shall return aborted if the device is in frozen mode.

Table 72: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action

requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

6.21. Security Erase Prepare- F3h

Table 73: Security erase prepare command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F3h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 74: Security erase prepare command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 75: Security erase prepare command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

6.22. Security Erase Unit- F4h

Table 76: Security erase unit command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 77: Security erase unit command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 78: Security erase unit command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is set.

Table 79: Security erase unit password information

Word	Content
0	Control Word Bit 0 Identifier 0= Compare User password 1= Compare Master password Bit 1 Erase mode 0=Normal Erase 1=Enhanced Erase Bit(15:2) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

6.23. Security Freeze Lock- F5h

Table 80: Security freeze lock for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 81: Security freeze lock for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 82: Security freeze lock for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECUIRTY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

6.24. Security Disable Password- F6h

Table 83: Security disable password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 84: Security disable password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

Table 85: Security disable password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							

LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

Description

The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. Table 13 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password if set.

Table 86: Security disable password command content

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit(15:1) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

6.25. Read Buffer- E4h

Table 87: Read Buffer command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							

LBA Mid	Na				
LBA High	Na				
Device	obs	Na	obs	DEV	Na
Command	E4h				

Device –

DEV shall specify the selected device.

Normal Output

Table 88: Read Buffer command for normal output information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

The device shall return command aborted if the command is not supported.

Table 89: Read Buffer command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one. The command prior to a READ BUFFER command shall be a WRITE BUFFER command.

Description

The READ BUFFER command enables the host to read the current contents of the device's sector buffer. The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

6.26. Write Buffer- E8h

Table 90: Write Buffer command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Command	E8h							

Device register –

DEV shall specify the selected device.

Normal Output

Table 91: Write Buffer command for normal output information

Register	7	6	5	4	3	2	1	0

Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register-

DEV shall specify the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be cleared to zero.

Error Outputs

The device shall return command aborted if the command is not supported.

Table 92: Write Buffer command for error output information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error register-

ABRT shall be set to one if this command is not supported. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register -

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

Prerequisites

DRDY set to one.

Description

This command enables the host to write the contents of one sector in the device's buffer. The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

7. Device Parameters

InnoDisk SATA Slim J80 device parameters listed in Table 94.

Table 93: InnoDisk SATA Slim J80 Device parameters

Capacity	Cylinders	Heads	Sectors	LBA
2GB				TBD
4GB	7801	16	63	7,863,408
8GB	15,603	16	63	15,728,824
16GB	16,383	16	63	31,457,280