INNODISK
Beyond your imagination

iCF 9000

Standard

the total solution for
industrial flash storage

Customer: _____

Customer Part Number: _____

InnoDisk Part Number: _____

InnoDisk Model Name: _____

Date: _____

InnoDisk Approver	Customer Approver

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REVISION HISTORY

Revision	Description	Date
Preliminary	Release First Version	Dec. 2011

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1. Introduction

The InnoDisk Industrial CompactFlash® 9000 Memory Card (iCF9000) products provide high capacity solid-state flash memory that electrically complies with the True IDE Mode that is electrically compatible with an IDE disk drive. The original CF form factor card can be used in any system that has a CF slot. Designed to replace traditional rotating disk drives, InnoDisk Industrial CompactFlash® 9000 Memory Cards are embedded solid-state data storage systems for mobile computing and the industrial work place. The Industrial CompactFlash® features an extremely lightweight, reliable, low-profile form factor. Industrial CompactFlash® 9000 (iCF9000) support advanced PIO (0-6), Multiword DMA (0-4), Ultra DMA (0-7) transfer mode, multi-sector transfers, and LBA addressing.

2. Features

The Industrial ATA products provide the following system features:

- Capacities: 2GB/4GB/8GB/16GB/32GB/64GB
- Fully compatible with CompactFlash® specification version 3.0
- Fully compatible with PC Card Standard.
- Fully compatible with the IDE standard interface, ATA Standard
- One access modes
  - True IDE Mode ONLY
- ECC (Error Correction Code) function: 8 bits/ per 512 byte
- +3.3V/+5V single power supply operation
- Support Auto Stand-by and Sleep Mode.
- Power Consumption
  - Quad:
    - ◆ 5V

      Active mode

      Read operation: TBD mA(max.)

      Write operation: TBD mA(max.)

      Power Down mode: TBD mA(max.)

    - ◆ 3.3V

      Active mode

      Read operation: TBD mA(Typ.)

      Write operation: TBD mA(Typ.)

      Power Down mode: TBD mA(max.)

- Support transfer modes: PIO(0-6), Multiword DMA (0-4) and Ultra DMA(0-7)
- MTBF 3,000,000 hours
- R/W performance:

- Quad:
  - Read: 95MBytes/s. (MAX)
  - Write: 90MBytes/s (MAX)

- Operating temperature range:
  - Standard Grade: 0°C ~ +70°C
  - Industrial Grade: -40°C ~ +85°C
- Storage temperature range: -55°C ~ +95°C

3. Pin Assignment

See Table 1 for iCF9000 pin assignments.

Table 1: iCF9000 Pin Assignments

True IDE Mode					
Pin No.	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**
1	GND		29	D13[1]	I/O
2	D03	I/O	30	D14[1]	I/O
3	D04	I/O	31	D15[1]	I/O
4	D05	I/O	32	-CS1[1]	I
5	D06	I/O	33	-VS1	GND
6	D07	I/O	34	-IORD[7]	I
7	-CS0	I			
8	A10[2]	GND			
9	-ATA SEL	GND	35	-IOWR[7]	I
10	A09[2]	GND			
11	A08[2]	GND	36	-WE[3]	I
12	A07[2]	GND	37	INTRQ	O
13	VCC	GND	38	VCC	
14	A06[2]	GND	39	-CSEL	I
15	A05[2]	GND	40	-VS2	NC
16	A04[2]	GND	41	-RESET	I
17	A03[2]	GND	42	IORDY[1]	O
18	A02	I			
19	A01	I			
20	A00	I	43	DMARQ	O
21	D00	I/O	44	-DMACK[6]	I
22	D01	I/O	45	-DASP	I/O
23	D02	I/O	46	-PDIAG	I/O
24	-IOCS16	NC	47	D08[1]	I/O
25	-CD2	GND	48	D09[1]	I/O
26	-CD1	GND	49	D10[1]	I/O
27	D11[1]	I/O	50	GND	
28	D12[1]	I/O			

Note:

1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 1-state signals not to consume current.
2) The signal should be grounded by the host.
3) The signal should be tied to VCC by the host.
4) The mode is optional for CF+ Cards, but required for CompactFlash® Storage Cards.
5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.
6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition
7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.
8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.
9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

4. Pin Description

Table 2 describes the pin descriptions for iCF9000

Table 2: iCF9000 Pin Description

Pin No.	Pin Name	I/O	Mode	Description
18,19,20	A2 – A0	I	True IDE Mode	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
46	-PDIAG	I/O	True IDE Mode	In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
45	-DASP	I/O	True IDE Mode	In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
26, 25	-CD1, -CD2	O	True IDE Mode	This signal is the same for all modes.
7, 32	-CS0, -CS1	I	True IDE Mode	In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register. While –DMACK is asserted, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits.
39	-CSEL	I	True IDE Mode	This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
2,3,4,5,6 31,30,29 28,27,49 48,47,23 22,21	D15 - D00	I/O	True IDE Mode	In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].
1, 50	GND	-	True IDE Mode	This signal is the same for all modes.

43	DMARQ	O	True IDE Mode	This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the host asserts -DMACK before negating DMARQ, and reasserting DMARQ if there is more data to transfer. DMARQ shall not be driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode.
34	-IORD	I	True IDE Mode	In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.
	-HDMARDY			In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an Ultra DMA transfer.
	HSTROBE			In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
35	-IOWR	I	True IDE Mode	In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.
	STOP			In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination

				of the Ultra DMA burst.
9	-ATA SEL	I	True IDE Mode	To enable True IDE Mode this input should be grounded by the host.
37	INTRQ	O	True IDE Mode	In True IDE Mode signal is the active high Interrupt Request to the host.
44	-DMACK	I	True IDE Mode	This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.
41	-RESET	I	True IDE Mode	In the True IDE Mode, this input pin is the active low hardware reset from the host.
13, 38	VCC	-	True IDE Mode	This signal is the same for all modes.
33, 40	-VS1, -VS2	O	True IDE Mode	This signal is the same for all modes.
42	IORDY	O	True IDE Mode	In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.
	-DDMARDY			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.
	DSTROBE			In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
36	-WE	I	True IDE Mode	In True IDE Mode, this input signal is not used and should be connected to VCC by the host.

24	-IOCS16	O	True IDE Mode	In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

5. Specifications

5.1 CE and FCC Compatibility

iCF9000 conforms to CE and FCC requirements.

5.2 RoHS Compliance

iCF9000 is fully compliant with RoHS directive.

5.3 Environmental Specifications

5.3.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C to +70°C
- Industrial Grade: -40°C to +85°C

Storage Temperature Range: -55°C to +95°C

5.3.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.3.3 Shock and Vibration

Table 3: Shock/Vibration Test for iCF9000

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2 KHz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500G, 3 axes	IEC 68-2-27

5.3.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various iCF9000 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 4: iCF9000 MTBF

Product	Condition	MTBF (Hours)
iCF9000	Telcordia SR-332 GB, 25°C	3,000,000

5.4 Mechanical Dimensions

Mechanical Dimension: 42.80±0.1/36.40±0.1/3.30±0.05mm (W/T/H)

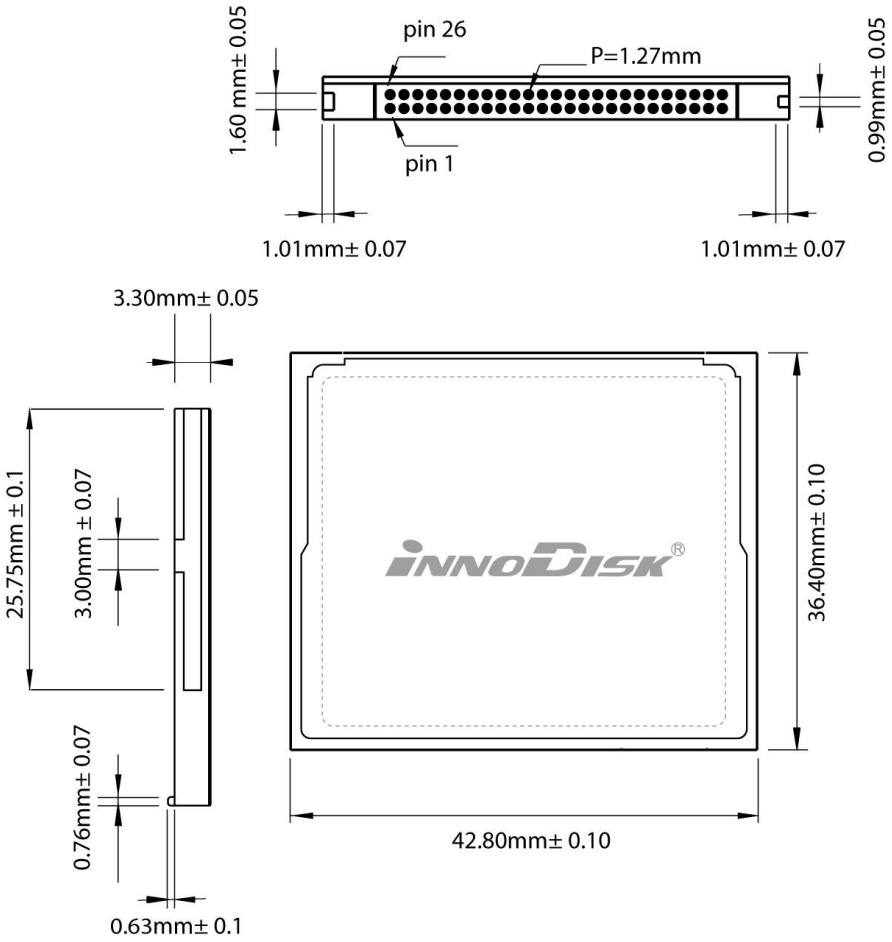

Figure 1: Mechanical Dimension of iCF9000

5.5 Electrical Specifications

TBD

6. Device Parameters

iCF9000 device parameters are listed in Table 91.

Table 5: Device parameters

Capacity	Cylinders	Heads	Sectors	LBA	Capacity(MB)
2GB	3,835	16	63	3,865,680	1,887.54
4GB	7,671	16	63	7,732,368	3,775.57
8GB	15,343	16	63	15,465,744	7,551.63
16GB	16,383	15	63	30,932,992	15,104
32GB	16,383	15	63	61,865,984	30,208

7. InnoDisk Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
	D	**C**	**1**	**M**	**-**	**0**	**2**	**G**	**D**	**7**	**1**	**A**	**C**	**1**	**Q**	**S**	**-**	**X**
Description	Disk	iCF9000			-	Capacity			Category			FW	Operation Temp.	Internal Control	Ch.	flash		Customized Code

Definition	
Code 1st (Disk)	**Code 12th (Firmware version)**
D : Disk	A: Standard FW
Code 2nd ~ 4th (Form Factor)	**Code 13th (Operation Temperature)**
C1M：CF, Type I,	C：Standard Grade (0 ~ +70 ℃)
	W：Industrial Grade (-40 ~ +85 ℃)
Code 6th ~8th (Capacity)	**Code 14th (Internal Control Code)**
02G：2GB	1: 1st PCB version, default setting
04G：4GB	**Code 15th (Channel of data transfer)**
08G：8GB	S: Single Channel
16G：16GB	D: Dual Channel
32G：32GB	Q: Quad Channel
	Code 16th (Flash Type)
Code 9th ~ 11th (Series)	S: Samsung SLC
D71：iCF 9000	**Code 18th (Customized Code)**